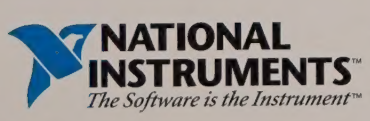
DAQ

PC-DIO-24 User Manual



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PC-DIO-24
User Manual

Digital I/O Board for the IBM PC/XT/AT

September 1995 Edition

Part Number 320288B-01

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This equipment generates and uses radio frequency energy and, if not installed and used in strict accordance with the instructions in this manual, may cause interference to radio and television reception. This equipment has been tested and found to comply with the following two regulatory agencies:

Federal Communications Commission

This device complies with Part 15 of the Federal Communications Commission (FCC) Rules for a Class A digital device. Operation is subject to the following two conditions:

1. This device may not cause harmful interference in commercial environments.

2. This device must accept any interference received, including interference that may cause undesired operation.

Canadian Department of Communications

This device complies with the limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications (DOC).

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de classe A prescrites dans le règlement sur le brouillage radioélectrique édicté par le ministère des communications du Canada.

Instructions to Users

These regulations are designed to provide reasonable protection against harmful interference from the equipment to radio reception in commercial areas. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

There is no guarantee that interference will not occur in a particular installation. However, the chances of interference are much less if the equipment is installed and used according to this instruction manual.

If the equipment does cause interference to radio or television reception, which can be determined by turning the equipment on and off, one or more of the following suggestions may reduce or eliminate the problem.

- Operate the equipment and the receiver on different branches of your AC electrical system.
- Move the equipment away from the receiver with which it is interfering.
- Reorient or relocate the receiver's antenna.
- Be sure that the equipment is plugged into a grounded outlet and that the grounding has not been defeated with a cheater plug.

Notice to user: Changes or modifications not expressly approved by National Instruments could void the user's authority to operate the equipment under the FCC Rules.

If necessary, consult National Instruments or an experienced radio/television technician for additional suggestions. The following booklet prepared by the FCC may also be helpful: *How to Identify and Resolve Radio-TV Interference Problems.* This booklet is available from the U.S. Government Printing Office, Washington, DC 20402, Stock Number 004-000-00345-4.

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About This Manual

This manual describes the mechanical and electrical aspects of the PC-DIO-24 and contains information concerning its operation and programming. The PC-DIO-24 is a 24-bit parallel, digital I/O interface designed around an 82C55A programmable peripheral interface (PPI). The PC-DIO-24 is a member of the National Instruments PC Series of PC I/O Channel expansion boards for the IBM PC computer family. These boards are designed for low-cost data acquisition and control for applications in laboratory testing, production testing, and industrial process monitoring and control.

This manual describes installation, basic programming considerations, and theory of operation for the PC-DIO-24. The example programs included are written in C.

Organization of This Manual

The PC-DIO-24 User Manual is organized as follows:

- Chapter 1, *Introduction*, describes the PC-DIO-24, lists what you need to get started, describes software programming choices, optional equipment, and custom cables, and explains how to unpack the PC-DIO-24.
- Chapter 2, *Configuration and Installation*, describes how to configure and install the PC-DIO-24, including I/O connector signal descriptions, handshake timing diagrams, and cabling instructions.
- Chapter 3, *Theory of Operation*, contains a functional overview of the PC-DIO-24 board and explains the operation of each functional unit making up the PC-DIO-24.
- Chapter 4, *Register-Level Programming*, describes in detail the address and function of each of the PC-DIO-24 control and status registers. This chapter also includes important information related to register-level programming the PC-DIO-24.
- Appendix A, *Specifications*, lists the specifications for the PC-DIO-24 board.
- Appendix B, *I/O Connector*, describes the pinout and signal names for the I/O connector on the PC-DIO-24.
- Appendix C, *OKI 82C55A Data Sheet*, contains the manufacturer data sheet for the OKI 82C55A (OKI Semiconductor) CMOS programmable peripheral interface. This interface is used on the PC-DIO-24 board.
- Appendix D, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products.
- The *Glossary* contains an alphabetical list and description of terms used in this manual, including abbreviations, acronyms, metric prefixes, mnemonics, symbols, and terms.

- The *Index* alphabetically lists the topics in this manual, including the page where you can find each one.

Conventions Used in This Manual

The following conventions are used in this manual.

bold	Bold text denotes menus, menu items, or dialog box buttons or options.
bold italic	Bold italic text denotes a note, caution, or warning.
italic	Italic text denotes emphasis, a cross reference, or an introduction to a key concept.
`monospace`	Lowercase text in this font denotes text or characters that are to be literally input from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, variables, filenames, and extensions, and for statements and comments taken from program code.
NI-DAQ	NI-DAQ refers to the NI-DAQ software for PC compatibles unless otherwise noted.
PC	PC refers to the IBM PC/XT, the IBM PC AT, and compatible computers unless otherwise noted.
SCXI	SCXI stands for Signal Conditioning eXtensions for Instrumentation and is a National Instruments product line designed to perform front-end signal conditioning for National Instruments plug-in DAQ boards.
<>	Angle brackets containing numbers separated by an ellipses represent a range, signal, or port (for example, ACH<0..7> stands for ACH0 through ACH7).

Abbreviations, acronyms, metric prefixes, mnemonics, and symbols are listed in the *Glossary*.

National Instruments Documentation

The *PC-DIO-24 User Manual* is one piece of the documentation set for your data acquisition (DAQ) system. You could have any of several types of manuals, depending on the hardware and software in your system. Use the different types of manuals you have as follows:

- *Getting Started with SCXI*—If you are using SCXI, this is the first manual you should read. It gives an overview of the SCXI system and contains the most commonly needed information for the modules, chassis, and software.

- Your SCXI hardware user manuals—If you are using SCXI, read these manuals next for detailed information about signal connections and module configuration. They also explain in greater detail how the module works and contain application hints.

- Your DAQ hardware user manuals—These manuals have detailed information about the DAQ hardware that plugs into or is connected to your computer. Use these manuals for hardware installation and configuration instructions, specification information about your DAQ hardware, and application hints.

- Software manuals—Examples of software manuals you may have are the LabVIEW and LabWindows®/CVI manual sets and the NI-DAQ manuals (a 4.6.1 or earlier version of NI-DAQ supports LabWindows for DOS). After you set up your hardware system, use either the application software (LabVIEW or LabWindows/CVI) manuals or the NI-DAQ manuals to help you write your application. If you have a large and complicated system, it is worthwhile to look through the software manuals before you configure your hardware.

- Accessory installation guides or manuals—If you are using accessory products, read the terminal block and cable assembly installation guides or accessory board user manuals. They explain how to physically connect the relevant pieces of the system. Consult these guides when you are making your connections.

- SCXI chassis manuals—If you are using SCXI, read these manuals for maintenance information on the chassis and installation instructions.

Related Documentation

The following documents contain information that you may find helpful as you read this manual:

- *IBM Personal Computer AT Technical Reference* manual

- *IBM Personal Computer XT Technical Reference* manual

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix D, *Customer Communication*, at the end of this manual.

Chapter 1
Introduction

This chapter describes the PC-DIO-24, lists what you need to get started, describes software programming choices, optional equipment, and custom cables, and explains how to unpack the PC-DIO-24.

About the PC-DIO-24

Thank you for purchasing the National Instruments PC-DIO-24. The PC-DIO-24 is a low cost, 24-bit parallel, digital I/O interface for the PC. An OKI 82C55A PPI controls the 24 bits of digital I/O. The 82C55A is very flexible and powerful when interfacing with peripheral equipment, can operate in either a unidirectional or bidirectional bus mode, and can generate interrupt request outputs. The 82C55A can be programmed for almost any 8-bit or 16-bit digital I/O application. All digital I/O is through a standard 50-pin male connector. The pin assignments for this connector are compatible with standard 24-channel digital I/O applications.

The PC-DIO-24 can be used in a wide range of digital I/O applications. With the PC-DIO-24, a PC can be interfaced to any of the following.

- Other computers
  - Another PC with a National Instruments PC-DIO-24 or AT-DIO-32F
  - IBM Personal System/2 with a National Instruments MC-DIO-24 or MC-DIO-32F
  - Apple Macintosh II with a National Instruments NB-DIO-24 or NB-DIO-32F
  - Any other computer with an 8-bit or 16-bit parallel interface
- Centronics-compatible printers and plotters
- Panel meters
- Instruments and test equipment with BCD readouts and/or controls
- Opto-isolated solid-state relays (SSRs) and I/O module mounting racks

Note: ***The PC-DIO-24 cannot sink sufficient current to drive the SSR-OAC-5 and SSR-OAC-5A output modules. However, it can drive the SSR-ODC-5 output module and all SSR input modules available from National Instruments.***

If you need to drive a SSR-OAC-5 or SSR-OAC-5A, you can either use a non-inverting digital buffer chip between the PC-DIO-24 and the SSR backplane, or you can use a DIO-23F or MIO Series board with appropriate connections (e.g., SC-205X and cables).

With the PC-DIO-24, the PC can serve as a digital I/O system controller for laboratory testing, production testing, and industrial process monitoring and control.

Detailed specifications of the PC-DIO-24 are in Appendix A, *Specifications*.

What You Need to Get Started

To set up and use your PC-DIO-24, you will need the following:

- ❑ PC-DIO-24 board
- ❑ *PC-DIO-24 User Manual*
- ❑ One of the following software packages and documentation:
  - NI-DAQ for PC compatibles
  - LabVIEW for Windows
  - LabWindows/CVI for Windows
- ❑ Your computer

Software Programming Choices

There are several options to choose from when programming your National Instruments DAQ and SCXI hardware. You can use LabVIEW, LabWindows/CVI, or NI-DAQ. A 4.6.1 or earlier version of NI-DAQ supports LabWindows for DOS.

LabVIEW and LabWindows/CVI Application Software

LabVIEW and LabWindows/CVI are innovative program development software packages for data acquisition and control applications. LabVIEW uses graphical programming, whereas LabWindows/CVI enhances traditional programming languages. Both packages include extensive libraries for data acquisition, instrument control, data analysis, and graphical data presentation.

LabVIEW features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW. The LabVIEW Data Acquisition VI Libraries are functionally equivalent to the NI-DAQ software.

LabWindows/CVI features interactive graphics, a state-of-the-art user interface, and uses the ANSI standard C programming language. The LabWindows/CVI Data Acquisition Library, a series of functions for using LabWindows/CVI with National Instruments DAQ hardware, is included with the NI-DAQ software kit. The LabWindows/CVI Data Acquisition libraries are functionally equivalent to the NI-DAQ software.

Using LabVIEW or LabWindows/CVI software will greatly reduce the development time for your data acquisition and control application.

NI-DAQ Driver Software

The NI-DAQ driver software is included at no charge with all National Instruments DAQ hardware. NI-DAQ is not packaged with SCXI or accessory products, except for the SCXI-1200. NI-DAQ has an extensive library of functions that you can call from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation, digital I/O, counter/timer operations, SCXI, RTSI, self-calibration, messaging, and acquiring data to extended memory.

NI-DAQ has both high-level DAQ I/O functions for maximum ease of use and low-level DAQ I/O functions for maximum flexibility and performance. Examples of high-level functions are streaming data to disk or acquiring a certain number of data points. An example of a low-level function is writing directly to registers on the DAQ device. NI-DAQ does not sacrifice the performance of National Instruments DAQ devices because it lets multiple devices operate at their peak performance.

NI-DAQ also internally addresses many of the complex issues between the computer and the DAQ hardware such as programming interrupts and DMA controllers. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Figure 1-1 illustrates the relationship between NI-DAQ and LabVIEW and LabWindows/CVI.

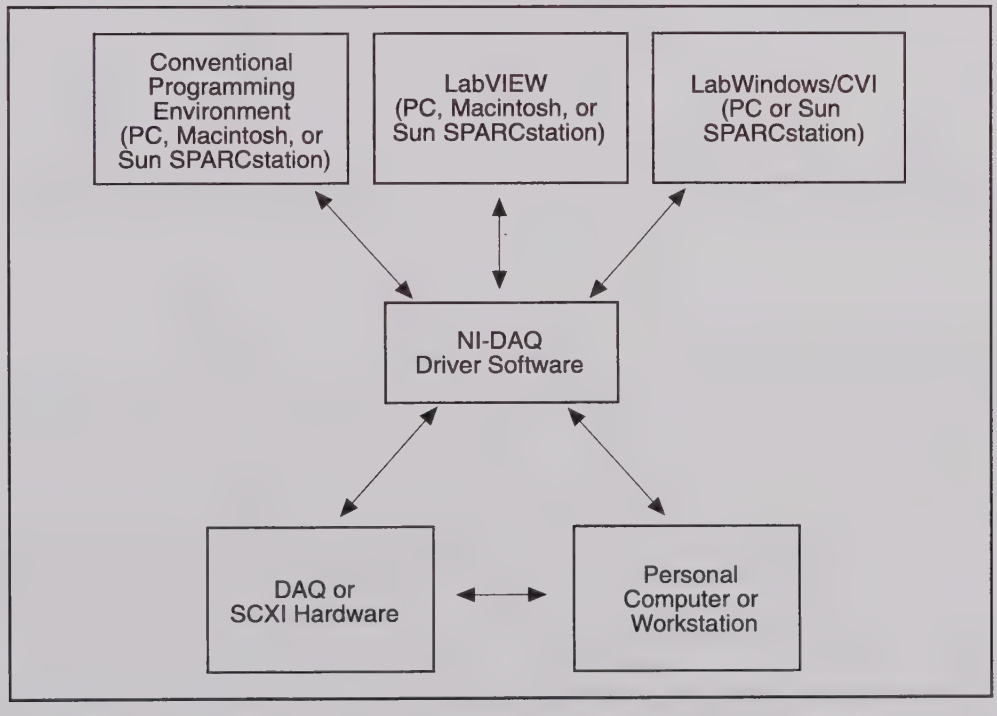

Conventional Programming Environment (PC, Macintosh, or Sun SPARCstation)
LabVIEW (PC, Macintosh, or Sun SPARCstation)
LabWindows/CVI (PC or Sun SPARCstation)
NI-DAQ Driver Software
DAQ or SCXI Hardware
Personal Computer or Workstation

Figure 1-1. The Relationship between the Programming Environment, NI-DAQ, and Your Hardware

Register-Level Programming

The final option for programming any National Instruments DAQ hardware is to write register-level software. Writing register-level programming software can be very time-consuming and inefficient, and is not recommended for most users.

Even if you are an experienced register-level programmer, consider using NI-DAQ, LabVIEW, or LabWindows/CVI to program your National Instruments DAQ hardware. Using the NI-DAQ, LabVIEW, or LabWindows/CVI software is easier than, and as flexible as, register-level programming, and can save weeks of development time.

Optional Equipment

National Instruments offers a variety of products to use with your PC-DIO-24 board, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies, shielded and ribbon
- Connector blocks, shielded and unshielded 50-pin screw terminals
- Signal conditioning eXtensions for Instrumentation (SCXI) modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output. With SCXI you can condition and acquire up to 3,072 channels.
- Low channel count signal conditioning modules, boards, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample and hole, and relays.

For more specific information about these products, refer to your National Instruments catalog or call the office nearest you.

Custom Cables

National Instruments offers cables and accessories for you to prototype your application or to use if you frequently change board interconnections.

If you want to develop your own cable, however, the following guidelines may be useful:

The PC-DIO-24 I/O connector is a 50-pin male ribbon-cable header. The manufacturer part numbers used by National Instruments for this header are as follows:

- Electronic Products Division/3M (part number 3596-5002)
- T&B/Ansley Corporation (part number 609-5007)

The mating connector for the PC-DIO-24 is a 50-position, polarized, ribbon socket connector with strain relief. National Instruments uses a polarized (keyed) connector to prevent inadvertent upside-down connection to the PC-DIO-24. Recommended manufacturer part numbers for this mating connector are as follows:

- Electronic Products Division/3M (part number 3425-7650)
- T&B/Ansley Corporation (part number 609-5041CE)

The standard ribbon cable (50-conductor, 28 AWG, stranded) that can be used with these connectors is as follows:

- Electronic Products Division/3M (part number 3365/50)
- T&B/Ansley Corporation (part number 171-50)

Recommended manufacturer part numbers for the 50-pin edge connector for connecting to a module rack with an edge connector are as follows:

- Electronic Products Division/3M (part number 3415-0001)
- T&B Ansley Corporation (part number 609-5015M)

A polarizing key can be plugged into these edge connectors to prevent inadvertent upside-down connection to the I/O module rack. The location of this key varies from rack to rack. Consult the specification for the rack you intend to use for the location of any polarizing key. The recommended manufacturer part numbers for this polarizing key are as follows:

- Electronic Products Division/3M (part number 3439-2)
- T&B Ansley Corporation (part number 609-0005)

If you plan to use the PC-DIO-24 for a communications application, you may need shielded cables to meet FCC requirements. The PC-DIO-24 I/O bracket has been designed so that the shield of the I/O cable can be grounded through the computer chassis when a mating connector such as the following is used:

- AMP Special Industries (part number 2-746483-2)

Many varieties of shielded ribbon cable are available to work with the mating connector listed previously. One type of shielded cable encloses a standard ribbon cable with a shielded jacket. Recommended manufacturers and the appropriate part numbers for this type of cable are as follows:

- Belden Electronic Wire and Cable (part number 9L28350)
- T&B/Ansley Corporation (part number 187-50)

Unpacking

Your PC-DIO-24 board is shipped in an antistatic package to prevent electrostatic damage to the board. Electrostatic discharge can damage several components on the board. To avoid such damage in handling the board, take the following precautions:

- Ground yourself via a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of your PC chassis before removing the board from the package.
- Remove the board from the package and inspect the board for loose components or any other sign of damage. Notify National Instruments if the board appears damaged in any way. *Do not* install a damaged board into your computer.
- *Never* touch the exposed pins of connectors.

Chapter 2
Configuration and Installation

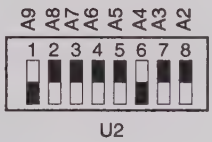
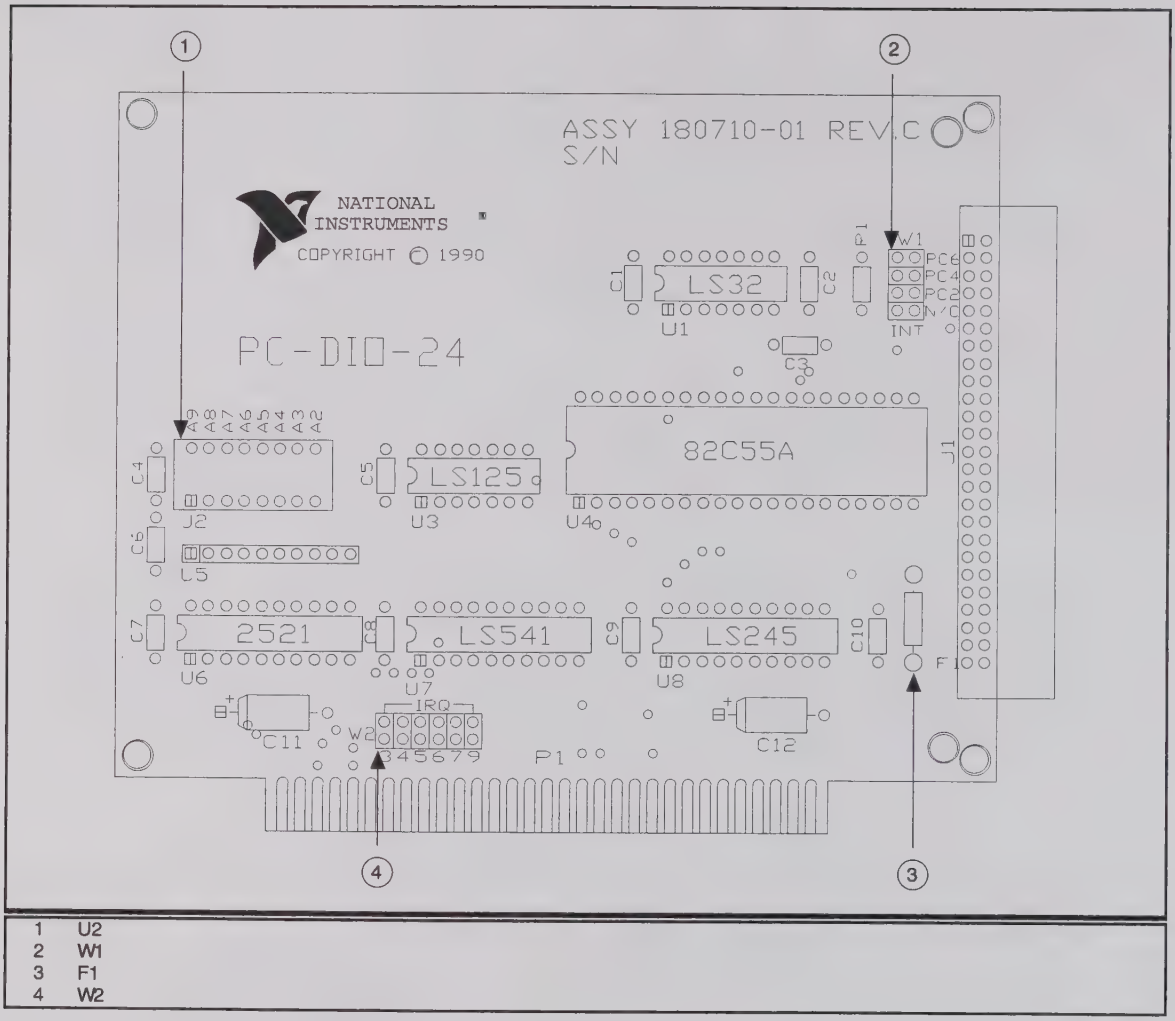
This chapter describes how to configure and install the PC-DIO-24, including I/O connector signal descriptions, handshake timing diagrams, and cabling instructions.

Board Configuration

The PC-DIO-24 contains one DIP switch and two jumpers to configure the base I/O address and interrupts, respectively. The PC-DIO-24 also contains one fuse to protect the +5 V power output. Figure 2-1 shows the location of jumper sets W1 and W2, DIP switch U2, and the fuse F1.

The PC-DIO-24 is configured at the factory to a base I/O address of hex 210, to use interrupt enable line PC4, and to use interrupt level 5. These settings (shown in Table 2-1) are suitable for most systems. However, if your system has other hardware at this base I/O address, interrupt enable line, or interrupt level, you need to change these settings on the PC-DIO-24 (as described in the following pages) or on the other hardware. Record your settings in the *PC-DIO-24 Hardware and Software Configuration Form* in Appendix D, *Customer Communication.*

Table 2-1. PC-DIO-24 Factory-Set Jumper and Switch Settings

Base I/O Address	Hex 210 (factory setting)	 (The black side indicates the side that is pushed down.)
Interrupt Enable Line	PC4 (factory setting)	W1: Row PC4
Interrupt Level	Interrupt level 5 selected (factory setting)	W2: IRQ5



1	U2
2	W1
3	F1
4	W2

Figure 2-1. PC-DIO-24 Parts Locator Diagram

Base I/O Address Settings

The base I/O address for the PC-DIO-24 is determined by the switches at position U2 (see Figure 2-1). The switches are set at the factory for the I/O address hex 210. With this default setting, the PC-DIO-24 uses the I/O address space hex 210 through 213.

Note: ***Verify that this space is not already used by other equipment installed in your computer. If any equipment in your computer uses this I/O address space, you must change the base I/O address for the PC-DIO-24 or for the other device.***

Each switch in U2 corresponds to one of the address lines A9 through A2. Thus, the range for possible base I/O address settings is hex 000 through 3FC. Base I/O address values hex 000 through 0FF are reserved for system use. Base I/O values hex 100 through 3FF are available on the I/O channel. A1 and A0 are used by the PC-DIO-24 to decode the onboard registers. On the

U2 DIP switches, press the side marked OFF to select a binary value of 1 for the corresponding address bit. Press the other side of the switch to select a binary value of 0 for the corresponding address bit. Figure 2-2 shows two possible switch settings. The black side indicates the side that is pushed down.

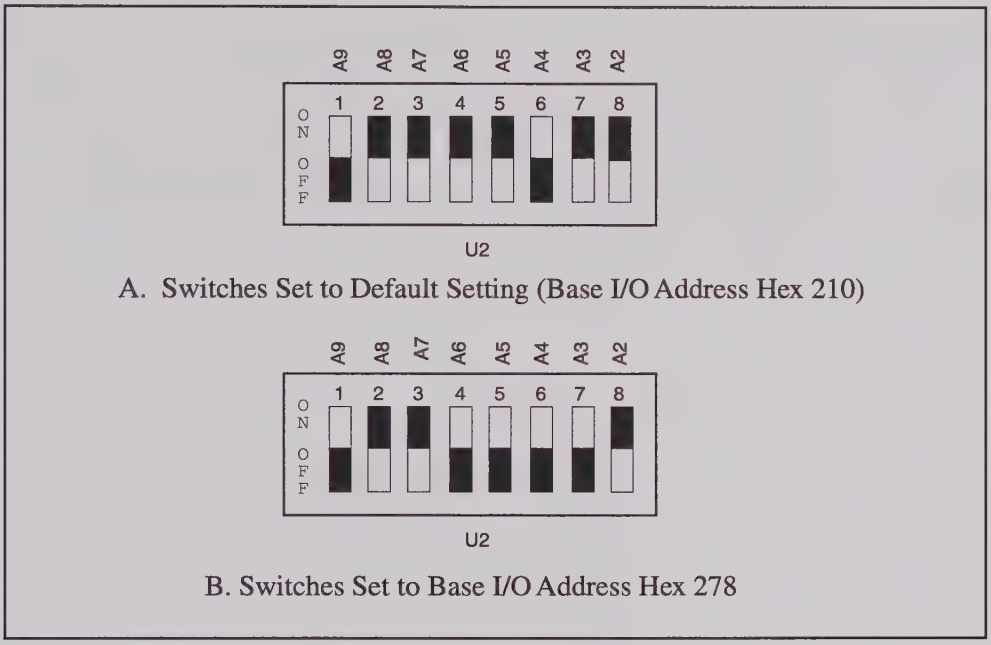

A9 A8 A7 A6 A5 A4 A3 A2
1 2 3 4 5 6 7 8
ON
OFF
U2
A. Switches Set to Default Setting (Base I/O Address Hex 210)
A9 A8 A7 A6 A5 A4 A3 A2
1 2 3 4 5 6 7 8
ON
OFF
U2
B. Switches Set to Base I/O Address Hex 278

Figure 2-2. Example Base I/O Address Switch Settings

Interrupt Selection

There are two sets of jumpers for interrupt selection on the PC-DIO-24 board. W1 is used for selecting the interrupt enable line. W2 is for selecting the interrupt level. The location of these jumpers is shown in Figure 2-1.

Interrupt Enable Settings

To enable interrupt requests from the PC-DIO-24, you must set jumper W1 to select PC2, PC4, or PC6 as the active low interrupt enable line. When the interrupt enable line is logic low, interrupts are enabled from the PC-DIO-24 board. Refer to Chapter 4, *Register-Level Programming*, for the suggested interrupt enable line setting for each digital I/O mode of operation. If W1 is set to N/C, all interrupt requests from the PC-DIO-24 are disabled. Figure 2-3 shows the possible jumper settings for W1. The board is shipped with this jumper set to PC4; therefore, interrupt requests from the board are enabled and controlled by PC4.

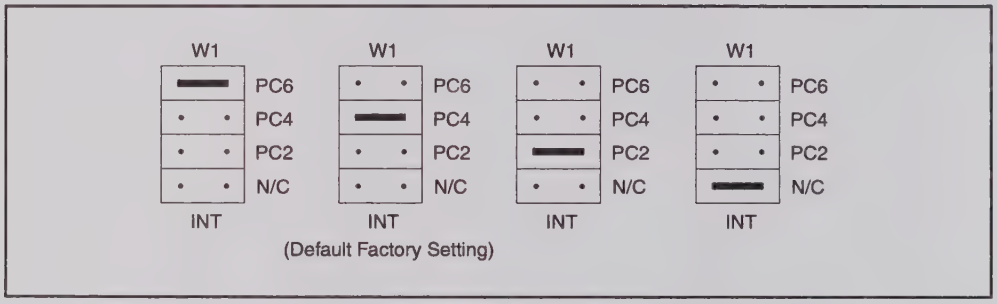


Figure 2-3. Jumper Settings–PC6, PC4, PC2, and N/C

Interrupt Level Settings

The PC-DIO-24 board can connect to any one of the six interrupt lines of the PC I/O Channel: IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, or IRQ9. You select the interrupt line by setting a jumper on W2. To use the interrupt capability of the board, you must select an interrupt line and place the jumper in the appropriate position. The default interrupt line is IRQ5. To change to another line, remove the jumper from IRQ5 and place it on the pins for another request line. Figure 2-4 shows the default factory setting for IRQ5.

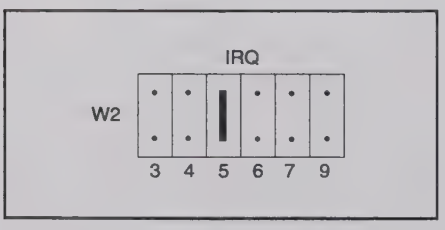


Figure 2-4. Interrupt Jumper Setting for IRQ5 (Factory Setting)

The PC-DIO-24 can share interrupt lines with other devices by using a tristate driver to drive its selected interrupt lines.

Installation

The PC-DIO-24 can be installed in any unused 8-bit or 16-bit expansion slot in your computer. After you make any necessary changes and verify the switch and jumper settings, record the settings in the *PC-DIO-24 Hardware and Software Configuration Form* in Appendix D, *Customer Communication*. You are now ready to install the PC-DIO-24.

The following are general installation instructions, but consult the user manual or technical reference manual of your personal computer for specific instructions and warnings.

1. Turn off your computer.
2. Remove the top cover or access port to the I/O channel.
3. Remove the expansion slot cover on the back panel of the computer.
4. Insert the PC-DIO-24 in an unused 8-bit or 16-bit slot. It may be a tight fit, but *do not* force the board into place.
5. Screw the mounting bracket of the PC-DIO-24 to the back panel rail of the computer.
6. Check the installation.
7. Replace the cover to the computer.

The PC-DIO-24 board is now installed and ready for operation.

Signal Connections

I/O Connector Pin Description

Figure 2-5 shows the pin assignments for the PC-DIO-24 digital I/O connector.

Warning: ***Connections that exceed any of the maximum ratings of input or output signals on the PC-DIO-24 may result in damage to the PC-DIO-24 board and to the PC. Maximum ratings for each signal are given in this chapter under the discussion of that signal. National Instruments is not liable for any damages resulting from any such signal connections.***

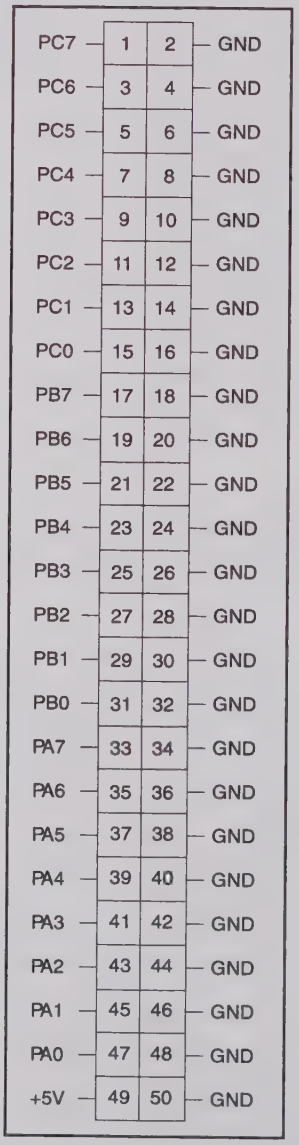

PC7 1 2 GND
PC6 3 4 GND
PC5 5 6 GND
PC4 7 8 GND
PC3 9 10 GND
PC2 11 12 GND
PC1 13 14 GND
PC0 15 16 GND
PB7 17 18 GND
PB6 19 20 GND
PB5 21 22 GND
PB4 23 24 GND
PB3 25 26 GND
PB2 27 28 GND
PB1 29 30 GND
PB0 31 32 GND
PA7 33 34 GND
PA6 35 36 GND
PA5 37 38 GND
PA4 39 40 GND
PA3 41 42 GND
PA2 43 44 GND
PA1 45 46 GND
PA0 47 48 GND
+5V 49 50 GND

Figure 2-5. Digital I/O Connector Pin Assignments

Signal Connection Descriptions

Pin	Signal Name	Description
1, 3, 5, 7, 9, 11, 13, 15	PC<7..0>	Port C—Bidirectional data lines for port C. PC7 is the MSB, PC0 the LSB.
17, 19, 21, 23, 25, 27, 29, 31	PB<7..0>	Port B—Bidirectional data lines for port B. PB7 is the MSB, PB0 the LSB.
33, 35, 37, 39, 41, 43, 45, 47	PA<7..0>	Port A—Bidirectional data lines for port B. PA7 is the MSB, PA0 the LSB.
49 (see note below)	+5 V	+5 Volts—This pin provides +5 VDC.
All even-numbered pins	GND	Ground—These signals are connected to the PC ground signal.
Note: ***Pin 49 is connected to the +5 V PC power supply via a 1 A fuse. A replacement fuse is available from Allied Electronics, part number 845-2007, or Littelfuse, part number 251001.***		

The absolute maximum voltage input rating is -0.5 to +5.5 V with respect to GND.

Port C Pin Assignments

The signals assigned to port C depend on the mode in which the 82C55A is programmed. In mode 0, port C is considered two 4-bit I/O ports. In modes 1 and 2, port C is used for status and handshaking signals with two or three I/O bits mixed in. Table 2-2 summarizes the signal assignments of port C for each programmable mode. See Chapter 4, *Register-Level Programming*, for register-level programming information.

Warning: ***During programming, note that each time a port is configured, output ports A and C are reset to 0, and output port B is undefined.***

Table 2-2. Port C Signal Assignments

Programming Mode	Group A				Group B			
	PC7	**PC6**	**PC5**	**PC4**	**PC3**	**PC2**	**PC1**	**PC0**
Mode 0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
Mode 1 Input	I/O	I/O	IBF_A	STB_A*	$INTR_A$	STB_B*	$IBFB_B$	$INTR_B$
Mode 1 Output	OBF_A*	ACK_A*	I/O	I/O	$INTR_A$	ACK_B*	OBF_B*	$INTR_B$
Mode 2	OBF_A*	ACK_A*	IBF_A	STB_A*	$INTR_A$	I/O	I/O	I/O
	* Indicates that the signal is active low.							

Timing Specifications

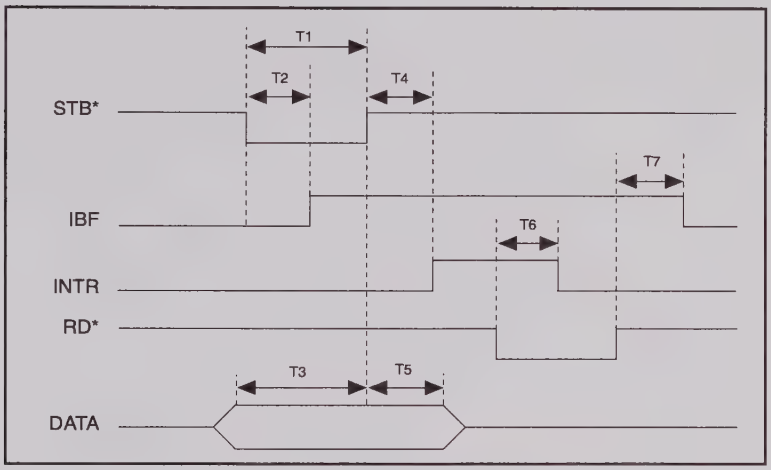
This section lists the timing specifications for handshaking with the PC-DIO-24. The handshaking lines STB* and IBF synchronize input transfers. The handshaking lines OBF* and ACK* synchronize output transfers.

The following signals are used in the timing diagrams on the subsequent pages.

Name	Signal Direction	Description
STB*	Input	Strobe Input—A low signal on this handshaking line loads data into the input latch.
IBF	Output	Input Buffer Full—A high signal on this handshaking line indicates that data has been loaded into the input latch. This is an input acknowledge signal.
ACK*	Input	Acknowledge Input—A low signal on this handshaking line indicates that the data written from the selected port has been accepted. This signal is a response from the external device that it has received the data from the PC-DIO-24.
OBF*	Output	Output Buffer Full—A low signal on this handshaking line indicates that data has been written from the selected port.
INTR	Output	Interrupt Request—This signal becomes high when the 82C55A is requesting service during a data transfer. The appropriate interrupt enable bits must be set to generate this signal.
RD*	Internal	Read Signal—This signal is the read signal generated from the control lines of the PC.
WR*	Internal	Write Signal—This signal is the write signal generated from the control lines of the PC.
DATA	Bidirectional	Data Lines at the Selected Port—This signal indicates when the data on the data lines at a selected port is or should be available.

Mode 1 Input Timing

The following figure illustrates the timing specifications for an input transfer in mode 1.

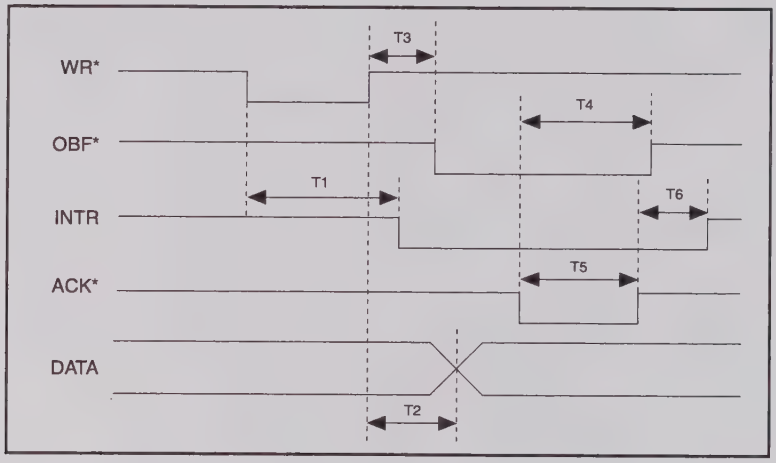


Name	Description	Minimum	Maximum
T1	STB* pulse width	100	–
T2	STB* = 0 to IBF = 1	–	150
T3	Data before STB* = 1	20	–
T4	STB* = 1 to INTR = 1	–	150
T5	Data after STB* = 1	50	–
T6	RD* = 0 to INTR = 0	–	200
T7	RD* = 1 to IBF = 0	–	150

All timing values are in nanoseconds.

Mode 1 Output Timing

The following figure illustrates the timing specifications for an output transfer in mode 1.

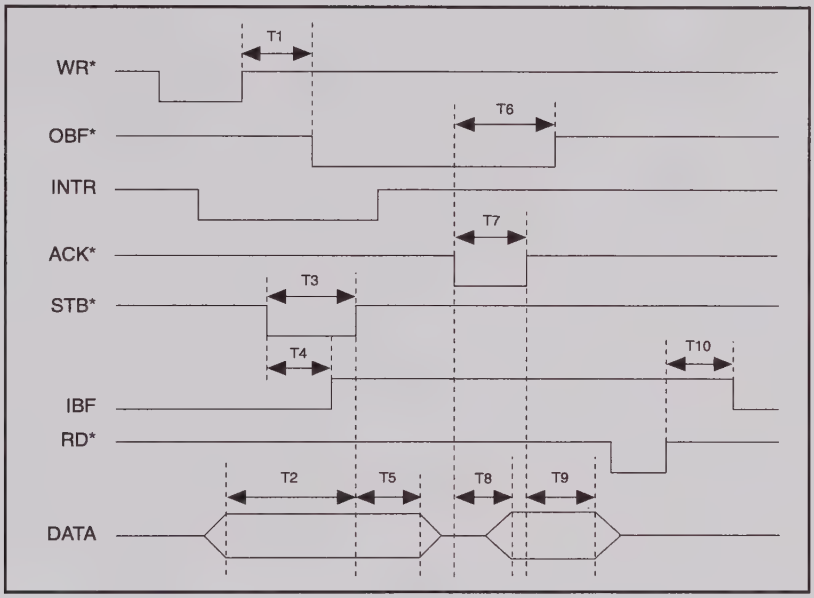


Name	Description	Minimum	Maximum
T1	WR* = 0 to INTR = 0	–	250
T2	WR* = 1 to output	–	200
T3	WR* = 1 to OBF* = 0	–	150
T4	ACK* = 0 to OBF* = 1	–	150
T5	ACK* pulse width	100	–
T6	ACK* = 1 to INTR = 1	–	150

All timing values are in nanoseconds.

Mode 2 Bidirectional Timing

The following figure illustrates the timing specifications for bidirectional transfers in mode 2.



Name	Description	Minimum	Maximum
T1	WR* = 1 to OBF* = 0	–	150
T2	Data before STB* = 1	20	–
T3	STB* pulse width	100	–
T4	STB* = 0 to IBF = 1	–	150
T5	Data after STB* = 1	50	–
T6	ACK* = 0 to OBF = 1	–	150
T7	ACK* pulse width	100	–
T8	ACK* = 0 to output	–	150
T9	ACK* = 1 to output float	20	250
T10	RD* = 1 to IBF = 0	–	150

All timing values are in nanoseconds.

Chapter 3
Theory of Operation

This chapter contains a functional overview of the PC-DIO-24 board and explains the operation of each functional unit making up the PC-DIO-24.

The block diagram in Figure 3-1 illustrates the key functional components of the PC-DIO-24 board.

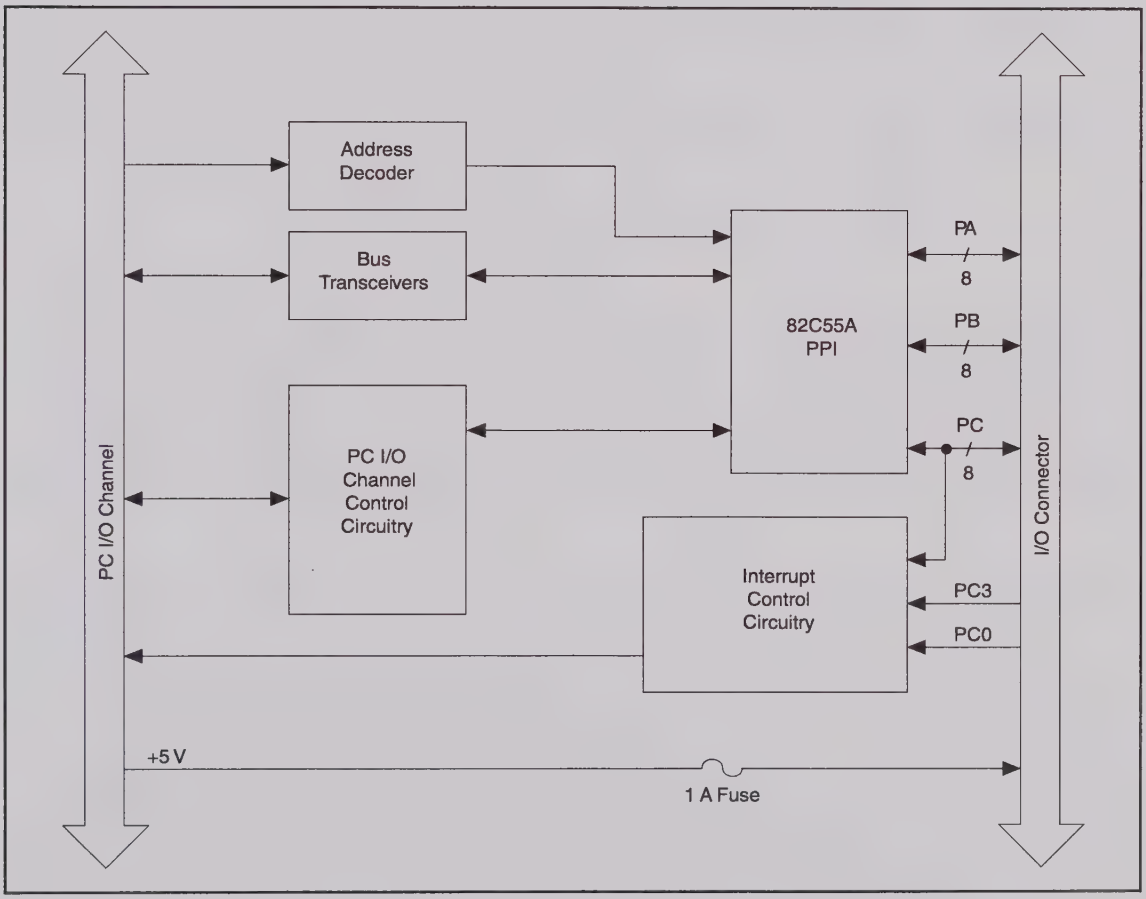


Figure 3-1. PC-DIO-24 Block Diagram

The PC I/O Channel consists of an address bus, a data bus, interrupt lines, and several control and support signals. Control and data transfers to the system microprocessor are asynchronous.

Address Decoder

The base address used by the board is determined by an onboard switch setting. The address on the PC I/O Channel bus is monitored by the address decoder. If the address on the bus matches the selected I/O base address of the board, the board is enabled and the corresponding register on the PC-DIO-24 is accessed.

Bus Transceivers

The bus transceivers control the sending and receiving of data lines to and from the PC I/O Channel.

PC I/O Channel Control Circuitry

This circuitry monitors and transmits the PC I/O Channel control and support signals. The control signals identify transfers as read or write, configuration or I/O, and 8-bit or 16-bit. The PC-DIO-24 only uses 8-bit transfers.

82C55A Programmable Peripheral Interface

The 82C55A PPI is the heart of the PC-DIO-24. This chip has 24 programmable I/O pins that represent three 8-bit ports—PA, PB, and PC. Each port can be programmed as an input or an output port. The 82C55A has three modes of operation—simple I/O (mode 0), strobed I/O (mode 1), and bidirectional I/O (mode 2). In modes 1 and 2, the three ports are divided into two groups—group A and group B. Each group has eight data bits and four control and status bits from port C (PC). Modes 1 and 2 use handshaking signals from port C to synchronize data transfers. Refer to Chapter 4, *Register-Level Programming*, or to Appendix C, *OKI 82C55A Data Sheet,* for more detailed information.

Interrupt Control Circuitry

The interrupt level used by the PC-DIO-24 is selected by the onboard jumper W2. Another onboard jumper, W1, is used to enable interrupts from the PC-DIO-24. The setting for W1 selects PC2, PC4, or PC6 as the active low interrupt enable signal. Selecting N/C for W1 disables interrupts from the PC-DIO-24. When the onboard jumpers are set to enable interrupts, the 82C55A can be programmed to generate an interrupt request by setting INTRA for group A or INTRB for group B. When interrupts are enabled for group A, an active high signal on the PC3 line generates an interrupt request. When interrupts are enabled for group B, an active high signal on the PC0 line generates an interrupt request.

Digital I/O Connector

All digital I/O is transmitted through a standard 50-pin male connector. The pin assignments for the I/O connector are compatible with standard 24-channel digital I/O applications. All even pins on this connector are attached to logic ground, and pin 49 is connected to +5 V through a protection fuse (F1), which is often required to operate I/O module mounting racks. See Chapter 2, *Configuration and Installation*, for additional information.

Chapter 4
Register-Level Programming

This chapter describes in detail the address and function of each of the PC-DIO-24 control and status registers. This chapter also includes important information related to register-level programming the PC-DIO-24.

The PC-DIO-24 is a parallel, digital I/O board designed around the OKI 82C55A integrated circuit. The 82C55A is a general-purpose peripheral interface containing 24 programmable I/O pins. These pins represent the three 8-bit I/O ports (A, B, and C) of the 82C55A. These ports can be programmed as two groups of 12 signals or as three individual 8-bit ports. This chapter includes register-level programming information for the PC-DIO-24, along with program examples written in C.

Note: ***If you plan to use a programming software package such as LabWindows/CVI or NI-DAQ with your PC-DIO-24 board, you need not read this chapter.***

Introduction

The three 8-bit ports are divided into two groups—group A and group B (two groups of 12 signals). One 8-bit configuration (or control) word determines the mode of operation for each group. The group A control bits configure port A<0..7> and the upper 4 bits (nibble) of port C<4..7>. The group B control bits configure port B<0..7> and the lower nibble of port C<0..3>. These configuration bits are defined later in this chapter.

82C55A Modes of Operation

The three basic modes of operation for the 82C55A are as follows:

- Mode 0 – Basic I/O
- Mode 1 – Strobed I/O
- Mode 2 – Bidirectional bus

The 82C55A also has a single bit set/reset feature for port C. The 8-bit control word also programs this function. For additional information, refer to Appendix C, *OKI 82C55A Data Sheet*.

Mode 0

This mode can be used for simple input and output operations for each of the ports. No handshaking is required; data is simply written to or read from a selected port.

Mode 0 has the following features:

- Two 8-bit ports (A and B) and two 4-bit ports (upper and lower nibble of port C).
- Any port can be input or output.
- Outputs are latched, but inputs are not latched.

Mode 1

This mode transfers data that is synchronized by handshaking signals. ports A and B use the eight lines of port C to generate or receive the handshake signals. This mode divides the ports into two groups (group A and group B):

- Each group contains one 8-bit data port (port A or port B) and one 4-bit control/data port (upper or lower nibble of port C).
- The 8-bit data ports can be either input or output, both of which are latched.
- The 4-bit ports are used for control and status of the 8-bit data ports.
- Interrupt generation and enable and/or disable functions are available.

Mode 2

This mode can be used for communication over a bidirectional 8-bit bus. Handshaking signals are used in a manner similar to mode 1. Interrupt generation and enable and/or disable functions are also available. Other features of this mode include the following:

- Used in group A only (port A and upper nibble of port C).
- One 8-bit bidirectional port (port A) and a 5-bit control status port (port C).
- Latched inputs and outputs.

Single Bit Set/Reset Feature

Any of the eight bits of port C can be set or reset with one control word. This feature generates status and control for port A and port B when operating in mode 1 or mode 2.

Register Map

The following table lists the address map for the PC-DIO-24. The registers PORTA, PORTB, PORTC, and CNFG are 8-bit registers in the 82C55A.

Table 4-1. PC-DIO-24 Address Map

Register	Offset Address (Hex)	Size	Type
PORTA	0x00	8-bit	Read-and-write
PORTB	0x01	8-bit	Read-and-write
PORTC	0x02	8-bit	Read-and-write
CNFG	0x03	8-bit	Write-Only

Note: ***A number preceded by 0x is a hexadecimal number.***

Register Descriptions

Figure 4-1 shows the two control-word formats used to completely program the 82C55A. The Control Word Flag determines which control-word format is being programmed. When the Control Word Flag is 1, bits 0 through 6 determine the I/O characteristics of the 82C55A ports and the mode in which they are operating (that is, mode 0, mode 1, or mode 2). When the Control Word Flag is 0, bits 3 through 0 determine the bit set/reset format of port C.

Warning: ***During programming, note that each time a port is configured, output ports A and C are reset to 0, and output port B is undefined.***

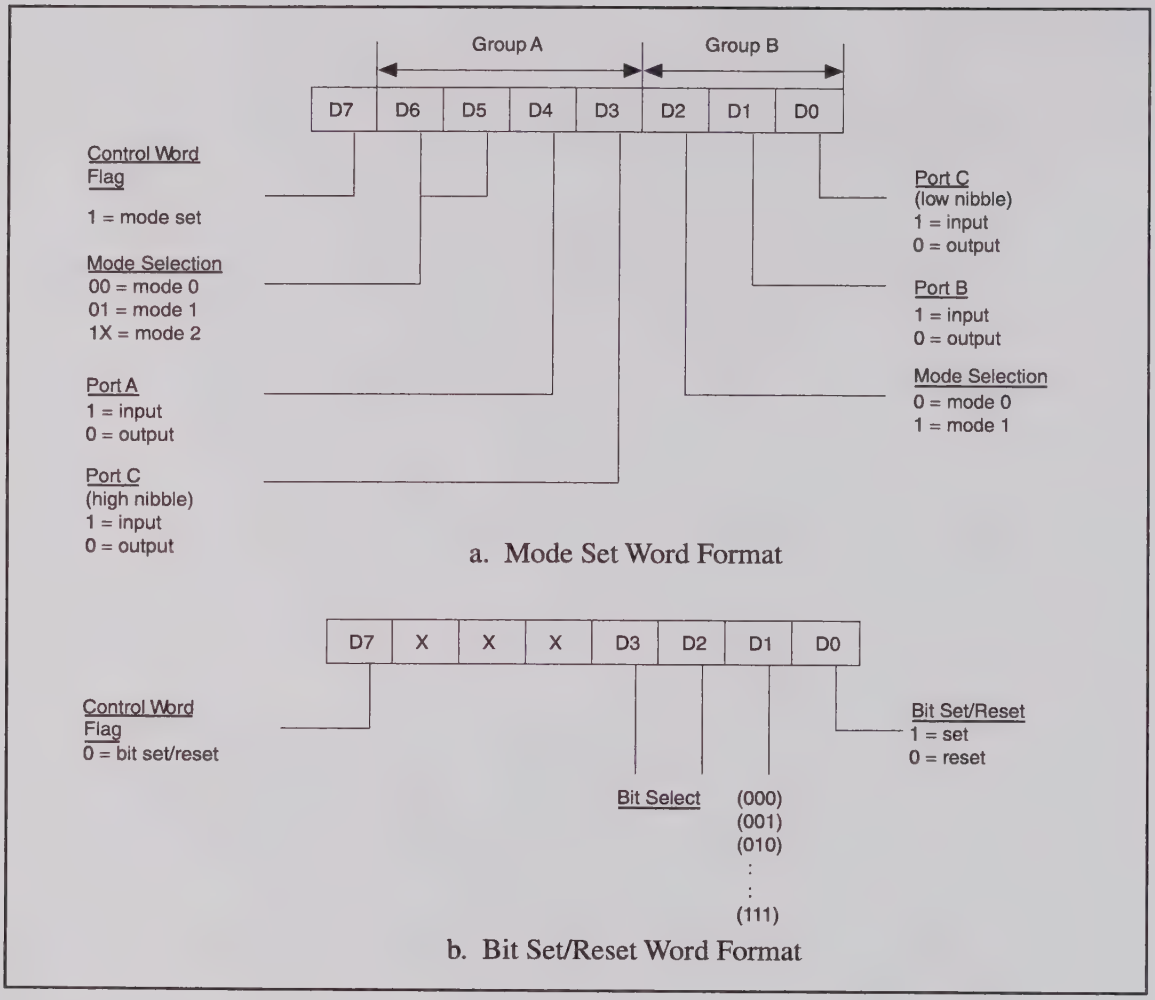


Figure 4-1. Control-Word Formats

Single Bit Set/Reset Feature

Table 4-2 shows the control words for setting or resetting each bit in port C. Notice that bit 7 of the control word is cleared when programming the set/reset option for the bits of port C.

Table 4-2. Port C Set/Reset Control Words

Number	Bit Set Control Word	Bit Reset Control Word	Bit Set or Reset in Port C
0	0xxx0001	0xxx0000	xxxxxxxn
1	0xxx0011	0xxx0010	xxxxxxnx
2	0xxx0101	0xxx0100	xxxxxnxx
3	0xxx0111	0xxx0110	xxxxnxxx
4	0xxx1001	0xxx1000	xxxnxxxx
5	0xxx1011	0xxx1010	xxnxxxxx
6	0xxx1101	0xxx1100	xnxxxxxx
7	0xxx1111	0xxx1110	nxxxxxxx

Programming Considerations

Mode 0–Basic I/O

Mode 0 can be used for simple I/O functions for each of the three ports with no handshaking. Each port can be assigned as an input or an output port. The 16 possible I/O configurations are shown in Table 4-3. Notice that bit 7 of the control word is set when programming the mode of operation for each port.

Table 4-3. Mode 0 I/O Configurations

	Control Word	Group A		Group B	
Number	**Bit 76543210**	**Port A**	**Port C[1]**	**Port B**	**Port C[2]**
0	10000000	Output	Output	Output	Output
1	10000001	Output	Output	Output	Input
2	10000010	Output	Output	Input	Output
3	10000011	Output	Output	Input	Input
4	10001000	Output	Input	Output	Output
5	10001001	Output	Input	Output	Input
6	10001010	Output	Input	Input	Output
7	10001011	Output	Input	Input	Input
8	10010000	Input	Output	Output	Output
9	10010001	Input	Output	Output	Input
10	10010010	Input	Output	Input	Output
11	10010011	Input	Output	Input	Input
12	10011000	Input	Input	Output	Output
13	10011001	Input	Input	Output	Input
14	10011010	Input	Input	Input	Output
15	10011011	Input	Input	Input	Input

[1] Upper nibble of port C
[2] Lower nibble of port C

Mode 0 Programming Example

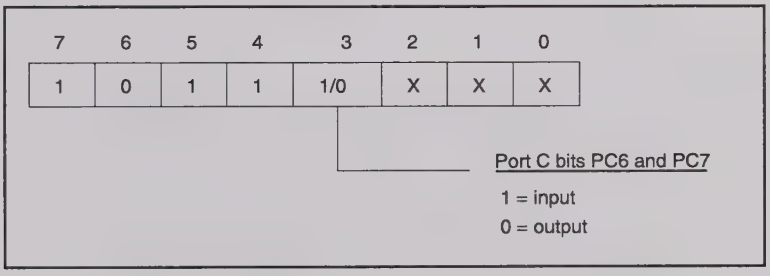
```
Main() {

#define BASE_ADDRESS        0x210      /* Board located at address 210 */
#define PORTAoffset         0x00       /* Offset for port A */
#define PORTBoffset         0x01       /* Offset for port B */
#define PORTCoffset         0x02       /* Offset for port C */
#define CNFGoffset          0x03       /* Offset for CNFG   */

register unsigned int porta, portb, portc, cnfg;
char valread;                          /* Variable to store data read from a
                                          port */

/*  Calculate register addresses. */
porta = BASE_ADDRESS + PORTAoffset;
portb = BASE_ADDRESS + PORTBoffset;
portc = BASE_ADDRESS + PORTCoffset;
cnfg  = BASE_ADDRESS + CNFGoffset;
```

```
/* EXAMPLE 1*/
outp(cnfg,0x80);                    /* Ports A, B, and C are outputs. */
outp(porta,0x12);                   /* Write data to port A. */
outp(portb,0x34);                   /* Write data to port B. */
outp(portc,0x56);                   /* Write data to port C. */

/* EXAMPLE 2*/
outp(cnfg,0x90);                    /* Port A is input; ports B and C are
                                       outputs. */
outp(portb,0x22);                   /* Write data to port B. */
outp(portc,0x55);                   /* Write data to port C. */
valread = inp(porta);               /* Read data from port A. */

/* EXAMPLE 3 */
outp(cnfg,0x82);                    /* Ports A and C are outputs; port B
                                       is an input. */

/* EXAMPLE 4 */
outp(cnfg,0x89);                    /* Ports A and B are outputs; port C
                                       is an input. */

}
```

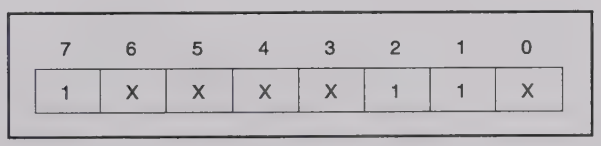
Mode 1–Strobed Input

In mode 1, the digital I/O bits are divided into two groups—group A and group B. Each of these groups contains one 8-bit port and one 4-bit control/data port. The 8-bit port can be either an input or an output, and the 4-bit port is used for control and status information for the 8-bit port. The transfer of data is synchronized by handshaking signals in the 4-bit port.

The control word written to the CNFG Register to configure port A for input in mode 1 is shown as follows. Bits PC6 and PC7 of port C can be used as extra input or output lines.



The control word written to the CNFG Register to configure port B for input in mode 1 is shown as follows. Notice that port B does not have extra input or output lines from port C.



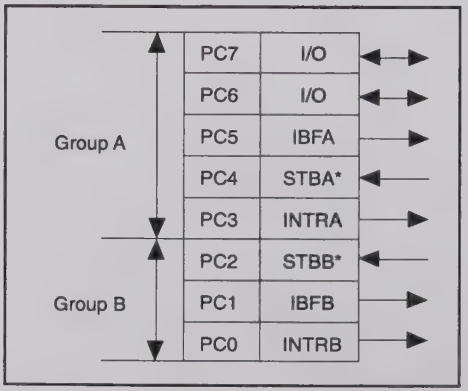
During a mode 1 data read transfer, the status of the handshaking lines and interrupt signals can be obtained by reading port C. The port C status-word bit definitions for an input transfer are shown as follows.

The following are the port C status-word bit definitions for input (port A and port B).

7	6	5	4	3	2	1	0
I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB

Bit	Name	Description
7–6	I/O	Input/Output—Extra I/O status lines when port A is in mode 1 input.
5	IBFA	Input Buffer Full for Port A—High indicates that data has been loaded into the input latch for port A.
4	INTEA	Interrupt Enable Bit for Port A—Enables interrupts from the 82C55A for port A. Controlled by bit set/reset of PC4.
3	INTRA	Interrupt Request Status for Port A—When INTEA is high and IBFA is high, this bit is high, indicating that an interrupt request is asserted.
2	INTEB	Interrupt Enable Bit for Port B—Enables interrupts from the 82C55A for port B. Controlled by bit set/reset of PC2.
1	IBFB	Input Buffer Full for Port B—High indicates that data has been loaded into the input latch for port B.
0	INTRB	Interrupt Request Status for Port B—When INTEB is high and IBFB is high, this bit is high, indicating that an interrupt request is asserted.

At the digital I/O connector, port C has the following pin assignments when in mode 1 input. Notice that the status of STBA* and STBB* are not included in the port C status word.

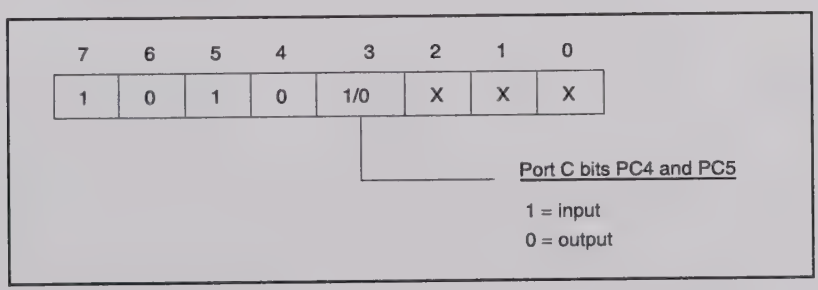


Mode 1 Input Programming Example

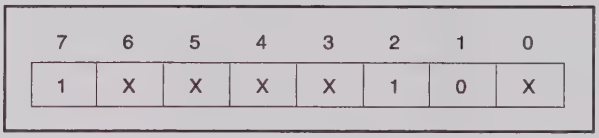
```
Main() {

#define BASE_ADDRESS        0x210      /* Board located at address 210. */
#define PORTAoffset         0x00       /* Offset for port A */
#define PORTBoffset         0x01       /* Offset for port B */
#define PORTCoffset         0x02       /* Offset for port C */
#define CNFGoffset          0x03       /* Offset for CNFG   */

register unsigned int porta, portb, portc, cnfg;
char valread;                          /* Variable to store data read from a
                                          port */

/*  Calculate register addresses. */

porta = BASE_ADDRESS + PORTAoffset;
portb = BASE_ADDRESS + PORTBoffset;
portc = BASE_ADDRESS + PORTCoffset;
cnfg  = BASE_ADDRESS + CNFGoffset;

/* EXAMPLE 1-port A input */

outp(cnfg,0xB0);                       /* Port A is an input in mode 1. */
while (!(inp(portc) & 0x20));          /* Wait until IBFA is set, indicating that
                                          data has been loaded in port A. */
valread = inp(porta);                  /* Read the data from port A. */

/* EXAMPLE 2-port B input */

outp(cnfg,0x86);                       /* Port B is an input in mode 1. */
while (!(inp(portc) & 0x02));          /* Wait until IBFB is set, indicating that
                                          data has been loaded in port B. */

valread = inp(portb);
}
```

Mode 1–Strobed Output

The control word written to the CNFG Register to configure port A for output in mode 1 is shown as follows. Bits PC4 and PC5 of port C can be used as extra input or output lines when port A uses mode 1 output.



The control word written to the CNFG Register to configure port B for output in mode 1 is shown as follows. Notice that port B does not have extra input or output lines from port C.



7	6	5	4	3	2	1	0
1	X	X	X	X	1	0	X

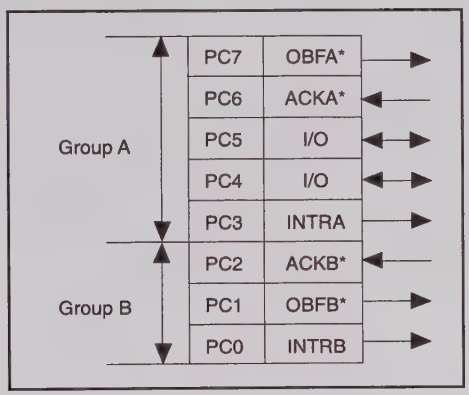
During a mode 1 data write transfer, the status of the handshaking lines and interrupt signals can be obtained by reading port C. Notice that the bit definitions are different for a write and a read transfer.

The following are the port C status-word bit definitions for output (port A and port B).

7	6	5	4	3	2	1	0
OBFA*	INTEA	I/O	I/O	INTRA	INTEB	OBFB*	INTRB

Bit	Name	Description
7	OBFA*	Output Buffer Full for Port A—Low indicates that the CPU has written data to port A.
6	INTEA	Interrupt Enable Bit for Port A—If this bit is high, interrupts are enabled from the 82C55A for port A. Controlled by bit set/reset of PC6.
5–4	I/O	Input/Output—Extra I/O status line when port A is in mode 1 output.
3	INTRA	Interrupt Request Status for Port A—When INTEA is high and OBFA* is high, this bit is high, indicating that an interrupt request is asserted.
2	INTEB	Interrupt Enable Bit for Port B—If this bit is high, interrupts are enabled from the 82C55A for port B. Controlled by bit set/reset of PC2.
1	OBFB*	Output Buffer Full for Port B—Low indicates that the CPU has written data out to port B.
0	INTRB	Interrupt Request Status for Port B—When INTEB is high and OBFB* is high, this bit is high, indicating that an interrupt request is asserted.

At the digital I/O connector, port C has the following pin assignments when in mode 1 output. Notice that the status of ACKA* and ACKB* is not included when port C is read.



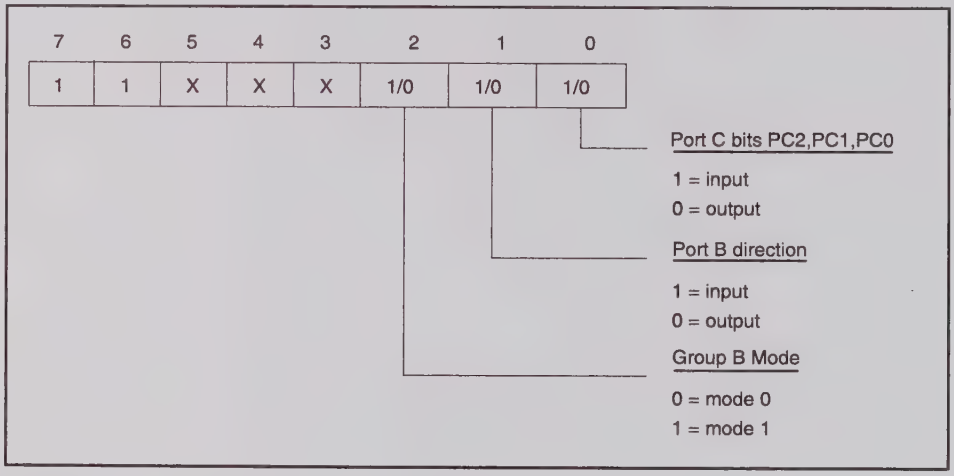
Mode 1 Output Programming Example

```
Main() {

#define BASE_ADDRESS        0x210      /* Board located at address 210. */
#define PORTAoffset         0x00       /* Offset for port A */
#define PORTBoffset         0x01       /* Offset for port B */
#define PORTCoffset         0x02       /* Offset for port C */
#define CNFGoffset          0x03       /* Offset for CNFG   */

register unsigned int porta, portb, portc, cnfg;
char valread;                          /* Variable to store data read from a
                                          port */

/*  Calculate register addresses. */
porta = BASE_ADDRESS + PORTAoffset;
portb = BASE_ADDRESS + PORTBoffset;
portc = BASE_ADDRESS + PORTCoffset;
cnfg  = BASE_ADDRESS + CNFGoffset;

/* EXAMPLE 1-port A output */

outp(cnfg,0xA0);                       /* Port A is an output in mode 1.*/
while (!(inp(portc) & 0x80));          /* Wait until OBFA* is set, indicating
                                          that the data last written to port A
                                          has been read.*/
outp(porta,0x12);                      /* Write data to port A. */

/* EXAMPLE 2-port B output */

outp(cnfg,0x84);                       /* Port B is an output in mode 1.*/
while (!(inp(portc) & 0x02));          /* Wait until OBFB* is set, indicating
                                          that the data last written to port B
                                          has been read.*/
outp(portb,0x34);                      /* Write the data to port B. */
}
```

Mode 2–Bidirectional Bus

Mode 2 has an 8-bit bus that can transfer both input and output without changing the configuration. The data transfers are synchronized with handshaking lines in port C. This mode uses only port A; however, port B can be used in either mode 0 or mode 1 while port A is configured for mode 2.

The control word written to the CNFG Register to configure port A as a bidirectional data bus in mode 2 is shown as follows. If port B is configured for mode 0, then PC2, PC1, and PC0 of port C can be used as extra input or output lines.



During a mode 2 data transfer, the status of the handshaking lines and interrupt signals can be obtained by reading port C. The port C status-word bit definitions for a mode 2 transfer are shown as follows.

The following are the port C status-word bit definitions for bidirectional data path (port A only).

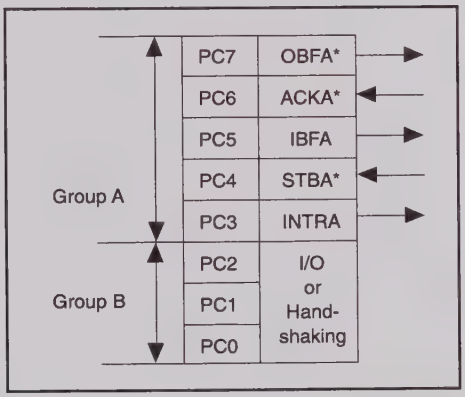
7	6	5	4	3	2	1	0
OBFA*	INTE1	IBFA	INTE2	INTRA	I/O	I/O	I/O

Bit	Name	Description
7	OBFA*	Output Buffer Full—Low indicates that the CPU has written data to port A.
6	INTE1	Interrupt Enable Bit for Output—If this bit is set, interrupts are enabled from the 82C55A for OBFA*. Controlled by bit set/reset of PC6.
5	IBFA	Input Buffer Full—High indicates that data has been loaded into the input latch of port A.

(continues)

Bit	Name	Description (continued)
4	INTE2	Interrupt Enable Bit for Input—If this bit is set, interrupts are enabled from the 82C55A for IBFA. Controlled by bit set/reset of PC4.
3	INTRA	Interrupt Request Status—If INTE1 is high and IBFA is high, this bit is high, indicating that an interrupt request is asserted for input transfers. If INTE2 is high and OBFA* is high, this bit is high, indicating that an interrupt request is asserted for output transfers.
2–0	I/O	Input/Output—Extra I/O status lines available if port B is not configured for mode 1.

At the digital I/O connector, port C has the following pin assignments when in mode 2.



Mode 2 Programming Example

```
Main() {

#define BASE_ADDRESS        0x210       /* Board located at address 210. */
#define PORTAoffset         0x00        /* Offset for port A */
#define PORTBoffset         0x01        /* Offset for port B */
#define PORTCoffset         0x02        /* Offset for port C */
#define CNFGoffset          0x03        /* Offset for CNFG */

register unsigned int porta, portb, portc, cnfg;
char valread;                           /* Variable to store data read from a
                                           port */

/*  Calculate register addresses. */
porta = BASE_ADDRESS + PORTAoffset;
portb = BASE_ADDRESS + PORTBoffset;
portc = BASE_ADDRESS + PORTCoffset;
cnfg  = BASE_ADDRESS + CNFGoffset;
```

```
/* EXAMPLE 1*/

outp(cnfg,0xC0);                        /* Port A is in mode 2. */
while (!(inp(portc) & 0x80));           /* Wait until OBFA* is set,
                                           indicating that the data last
                                           written to port A has been
                                           read.*/
outp(porta,0x67);                       /* Write the data to port A. */
while (!(inp(portc) & 0x20));           /* Wait until IBFA is set, indicating
                                           that data is available in port A to
                                           be read. */
valread = inp(porta);                   /* Read data from port A. */
}
```

Interrupt Programming Examples

The following examples show the process required to enable interrupts for several different operating modes. The interrupt handling routines and interrupt installation routines are not included. See the *IBM Personal Computer AT Technical Reference* manual for additional information.

```
Main() {

#define BASE_ADDRESS        0x210       /* Board located at address 210. */
#define PORTAoffset         0x00        /* Offset for port A */
#define PORTBoffset         0x01        /* Offset for port B */
#define PORTCoffset         0x02        /* Offset for port C */
#define CNFGoffset          0x03        /* Offset for CNFG */

register unsigned int porta, portb, portc, cnfg;
char valread;                           /* Variable to store data read from a
                                           port */

/* Calculate register addresses. */
porta = BASE_ADDRESS + PORTAoffset;
portb = BASE_ADDRESS + PORTBoffset;
portc = BASE_ADDRESS + PORTCoffset;
cnfg  = BASE_ADDRESS + CNFGoffset;

/* EXAMPLE 1-Set up interrupts for mode 1 input for port A.  Select PC6 as the
interrupt enable bit. */

outp(cnfg,0xB0);                    /* Port A is an input in mode 1. */
outp(cnfg,0x09);                    /* Set PC4 to enable interrupts from
                                       82C55A. */
outp(cnfg,0x0C);                    /* Clear PC6 to enable interrupts. */

/* EXAMPLE 2-Set up interrupts for mode 1 input for port B.  Select PC6 as the
interrupt enable bit. */

outp(cnfg,0x86);                    /* Port B is an input in mode 1. */
outp(cnfg,0x05);                    /* Set PC2 to enable interrupts from
                                       82C55A. */
outp(cnfg,0x0C);                    /* Clear PC6 to enable interrupts. */
```

```
/* EXAMPLE 3-Set up interrupts for mode 1 output for port A.  Select PC4 as
the interrupt enable bit. */

outp(cnfg,0xA0);                    /* Port A is an output in mode 1. */
outp(cnfg,0x0D);                    /* Set PC6 to enable interrupts from
                                       82C55A. */
outp(cnfg,0x0C);                    /* Clear PC4 to enable interrupts. */

/* EXAMPLE 4-Set up interrupts for mode 1 output for port B.  Select PC4 as
the interrupt enable bit. */

outp(cnfg,0x84);                    /* Port B is an output in mode 1. */
outp(cnfg,0x05);                    /* Set PC2 to enable interrupts from
                                       82C55A. */
outp(cnfg,0x08);                    /* Clear PC4 to enable interrupts. */

/* EXAMPLE 5-Set up interrupts for mode 2 output transfers.  Select PC2 as the
interrupt enable bit. */

outp(cnfg,0xC0);                    /* mode 2 output */
outp(cnfg,0x0D);                    /* Set PC6 to enable interrupts from
                                       82C55A. */
outp(cnfg,0x04);                    /* Clear PC2 to enable interrupts. */

/* EXAMPLE 6-Set up interrupts for mode 2 input transfers.  Select PC2 as the
interrupt enable bit. */

outp(cnfg,0xD0);                    /* mode 2 input */
outp(cnfg,0x09);                    /* Set PC4 to enable interrupts from
                                       82C55A. */
outp(cnfg,0x04);                    /* Clear PC2 to enable interrupts. */
}
```

Interrupt Handling

A jumper setting on the PC-DIO-24 selects the signal that is used for the interrupt enable signal. If jumper W1 is set to N/C, interrupts are disabled. Jumper W1 can be used to select PC2, PC4, or PC6 as the active low interrupt enable signal. For example, if PC2 is selected, interrupts are enabled if PC2 is logic low. If PC2 is logic high, interrupts from the PC-DIO-24 are disabled. The following table summarizes which signal should be used as the interrupt enable for all mode combinations.

Table 4-4. Interrupt Enable Signals for All Mode Combinations

Port A Mode 2 Output	Port A Mode 2 Input	Port B Mode 1 Output	Port B Mode 1 Input	Port A Mode 1 Output	Port A Mode 1 Input	Port B Mode 0	Port A Mode 0	Interrupt Enable Bit
No	No	No	No	No	No	Yes	Yes	N/C
No	No	No	No	No	Yes	Yes	No	PC6, PC2
No	No	No	No	Yes	No	Yes	No	PC4, PC2
No	No	No	Yes	No	No	No	Yes	PC6, PC4
No	No	No	Yes	No	Yes	No	No	PC6
No	No	No	Yes	Yes	No	No	No	PC4
No	No	Yes	No	No	No	No	Yes	PC6, PC4
No	No	Yes	No	No	Yes	No	No	PC6
No	No	Yes	No	Yes	No	No	No	PC4
No	Yes	No	No	No	No	Yes	No	PC2
No	Yes	No	Yes	No	No	No	No	N/C
No	Yes	Yes	No	No	No	No	No	N/C
Yes	No	No	No	No	No	Yes	No	PC2
Yes	No	No	Yes	No	No	No	No	N/C
Yes	No	Yes	No	No	No	No	No	N/C

The recommended jumper settings for W1 are as follows.

- PC6 — If port A is in mode 1 input.
- PC4 — If port A is in mode 1 output.
- PC2 — If port A is in mode 2 (port B is not in mode 1).

To enable interrupts from the PC-DIO-24, select PC2, PC4, or PC6 as the active low interrupt enable signal. Initially, set the selected bit high to disable unwanted interrupts.

Program the PC-DIO-24 for the I/O mode desired. To enable interrupts from the 82C55A, set either the INTEA or the INTEB bit to enable interrupts from port A or port B, respectively. In mode 2, set either INTE1 or INTE2 for interrupts on input or output transfers. After interrupts have been enabled from the 82C55A, clear the selected interrupt enable bit to enable interrupts from the PC-DIO-24.

An external signal can be used to interrupt the PC-DIO-24 when port A or port B is in mode 0. Select PC2, PC4, or PC6 as the interrupt enable bit and clear the selected bit to enable interrupts. Connect the external signal that should trigger an interrupt to either PC3 or PC0. When the external signal becomes logic high, an interrupt request occurs. To disable the external signal interrupt, set the selected interrupt enable bit to logic high.

Appendix A
Specifications

This appendix lists the specifications for the PC-DIO-24 board. These specifications are typical at 25° C, unless otherwise stated. The operating temperature range is 0° to 70° C.

Digital I/O

Number of channels ..... 24 I/O
Compatibility ..... TTL
Absolute max voltage input rating ..... -0.5 to +5.5 V with respect to GND
Handshaking ..... Requires 1 port
Power-on state ..... Configured as inputs
Data transfers ..... Interrupts, programmed I/O

Digital Logic Levels

Input Signals

Odd-numbered pins 1–47 .....

Level	Min	Max
Input logic high voltage	2.2 V	5.3 V
Input logic low voltage	-0.3 V	0.8 V
Input current ($0 < V_{in} < 5$ V)	-1.0 µA	1.0 µA

Output Signals

Pin 49 (at +5 V) ..... 0.25 A max

Odd-numbered pins 1–47 .....

Level	Min	Max
Output high voltage (I_{out} = -2.5 mA)	3.7 V	5.0 V
Output low voltage (I_{out} = 2.5 mA)	0.0 V	0.4 V
Output current (V_{OL} = 0.5 V)	4 mA	—
Output current (V_{OH} = 2.7 V)	4 mA	—

Environment

Operating Temperature ..... 0° to 70° C
Storage Temperature ..... -55° to 150° C
Relative humidity ..... 5% to 90% noncondensing

Physical

Dimensions ..... 17.5 by 9.9 cm (6.9 in. by 3.9 in.)
I/O connector ..... 50-pin male ribbon-cable connector

Power Requirement (from PC I/O Channel)

Typ power ..... 0.10 A at 5 VDC (±10%)
Max power ..... 0.16 A at 5 VDC (±10%)

Transfer Rates

The maximum average transfer rates for the PC-DIO-24 are shown as follows. The code used to make the measurements follows the table. The assembly language code was assembled as inline assembly C code using version 8.00 of the Microsoft Optimizing C Compiler. The C code was compiled using version 8.00 of the Microsoft Optimizing C Compiler.

Table A-1. Maximum Average Transfer Rates for the PC-DIO-24

Bus	CPU	CPU Speed	Assembly	C
AT (ISA16)	486DX4	100 MHz	410 kbytes/s	330 kbytes/s

Assembly language code:

```
        mov     cx, 64                  ; Count out 64 transfers
        mov     dx, 0180h               ; The port to access
    loop:
        lodsb                           ; Assume ds:si points to buffer of data
        out     dx, al                  ; Send the data
        add     dx, 0014h               ; Add offset to base address for Ireg1
        in      al, dx                  ; Dummy read from Ireg1
        sub     dx, 0014h               ; Restore base address
                                        ; The previous four lines are not
                                        ; necessary for measuring transfer rates
        dec     cx                      ; Decrement the loop counter
        jnz     short loop              ; See if we need to loop
```

C code:

```
    address = 0x0180;                   /* The port address */
    ireg1address = address + 0x0014;
    for (i = 0; i < 64; i++) {          /* Loop 64 times */
        outp(address, *data++);         /* Send data */
        inp(ireg1address);
    }
```

Appendix B
I/O Connector

This appendix describes the pinout and signal names for the I/O connector on the PC-DIO-24.

Figure B-1 shows the PC-DIO-24 digital I/O connector.

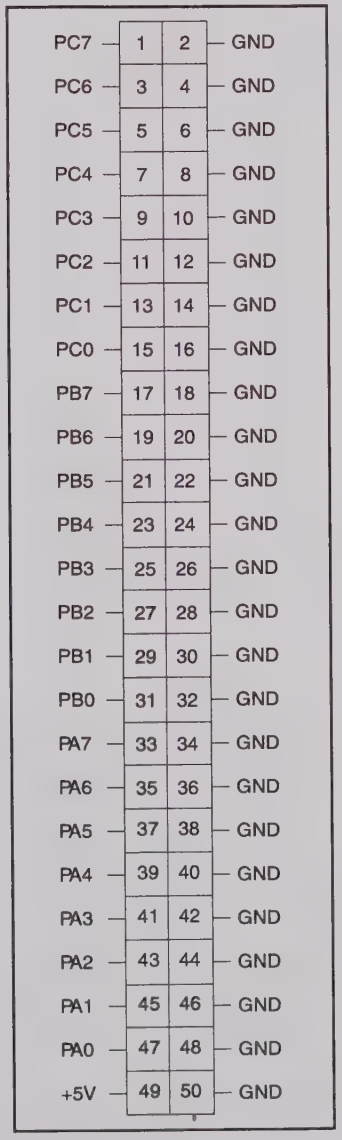

PC7 1 2 GND
PC6 3 4 GND
PC5 5 6 GND
PC4 7 8 GND
PC3 9 10 GND
PC2 11 12 GND
PC1 13 14 GND
PC0 15 16 GND
PB7 17 18 GND
PB6 19 20 GND
PB5 21 22 GND
PB4 23 24 GND
PB3 25 26 GND
PB2 27 28 GND
PB1 29 30 GND
PB0 31 32 GND
PA7 33 34 GND
PA6 35 36 GND
PA5 37 38 GND
PA4 39 40 GND
PA3 41 42 GND
PA2 43 44 GND
PA1 45 46 GND
PA0 47 48 GND
+5V 49 50 GND

Figure B-1. PC-DIO-24 I/O Connector

Detailed signal specifications are included in Chapter 2, *Configuration and Installation.*

Appendix C
OKI 82C55A Data Sheet*

This appendix contains the manufacturer data sheet for the OKI 82C55A (OKI Semiconductor)* CMOS programmable peripheral interface. This interface is used on the PC-DIO-24 board.

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OKI Semiconductor Data Book *Microprocessor,* Seventh Edition, March 1993.

OKI semiconductor

MSM82C55A-2RS/GS/VJS

CMOS PROGRAMMABLE PERIPHERAL INTERFACE

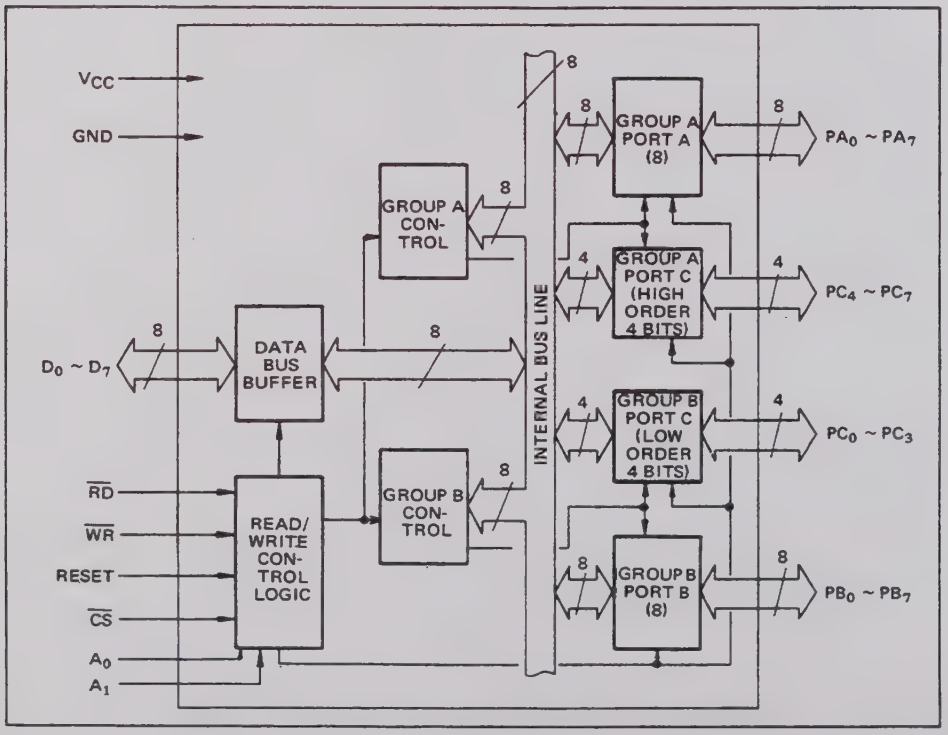
GENERAL DESCRIPTION

The MSM82C55A is a programmable universal I/O interface device which operates as high speed and on low power consumption due to 3 μ silicon gate CMOS technology. It is the best fit as an I/O port in a system which employs the 8-bit parallel processing MSM80C85A CPU. This device has 24-bit I/O pins equivalent to three 8-bit I/O ports and all inputs/outputs are TTL interface compatible.

FEATURES

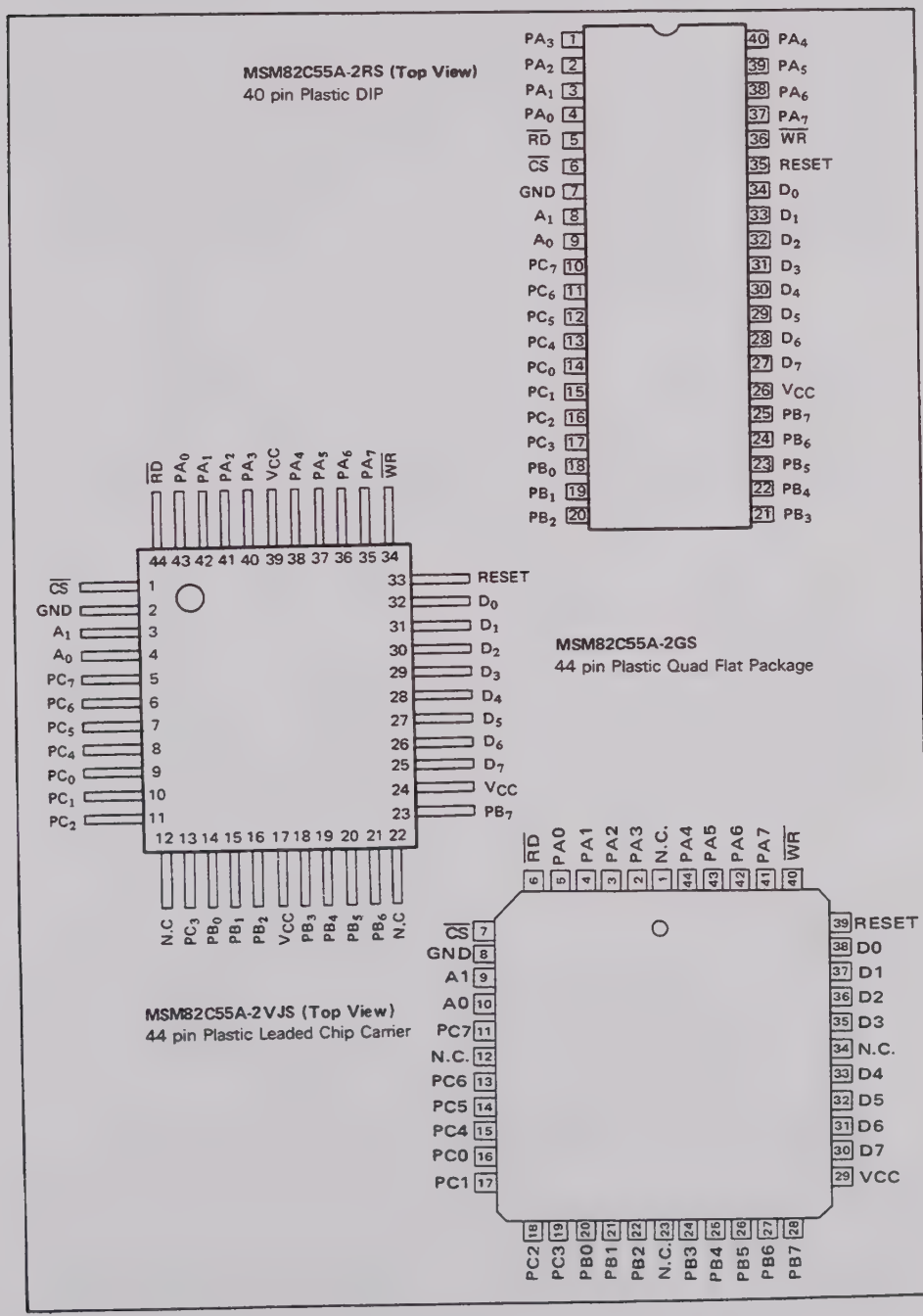
- High speed and low power consumption due to 3 μ silicon gate CMOS technology
- 3 V to 6 V single power supply
- Full static operation
- Programmable 24-bit I/O ports
- Bidirectional bus operation (Port A)
- Bit set/reset function (Port C)
- TTL compatible
- Compatible with 8255A-5
- 40 pin Plastic DIP (DIP40-P-600)
- 44 pin PLCC (QFJ44-P-S650)
- 44 pin-V Plastic QFP (QFP44-P-910-VK)
- 44 pin-VI Plastic QFP (QFP44-P-910-VIK)

CIRCUIT CONFIGURATION



I/O·MSM82C55A-2RS/GS/VJS

PIN CONFIGURATION



■ I/O·MSM82C55A-2RS/GS/VJS ■

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits			Unit
			MSM82C55A-2RS	MSM82C55A-2GS	MSM82C55A-2VJS	
Ssupply Voltage	V_{CC}	Ta = 25°C with respect to GND	−0.5 to +7			V
Input Voltage	V_{IN}		−0.5 to V_{CC} + 0.5			V
Output Voltage	V_{OUT}		−0.5 to V_{CC} + 0.5			V
Storage Temperature	T_{stg}	—	−55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	1.0	0.7	1.0	W

OPERATING RANGE

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	3 to 6	V
Operating Temperature	T_{OP}	–40 to 85	°C

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	–40	+25	+85	°C
"L" Input Voltage	V_{IL}	–0.3		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} +0.3	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		MSM82C55A-2			Unit
				Min.	Typ.	Max.	
"L" Output Voltage	V_{OL}	I_{OL} = 2.5 mA	V_{CC} = 4.5V to 5.5V Ta = −40°C to +85°C (C_L = 0pF)			0.4	V
"H" Output Voltage	V_{OH}	I_{OH} = −40 μA		4.2			V
		I_{OH} = −2.5 mA		3.7			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$		−1		1	μA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$		−10		10	μA
Supply Current (standby)	I_{CCS}	$\overline{CS} \geqq V_{CC}$ −0.2V $V_{IH} \geqq V_{CC}$ −0.2V $V_{IL} \leqq$ 0.2V			0.1	10	μA
Average Supply Current (active)	I_{CC}	I/O wire cycle 82C55A-2 ... 8MHzCPU timing				8	mA

AC CHARACTERISTICS

(V_{CC} = 4.5 to 5.5V, Ta = –40 to +80°C)

Parameter	Symbol	MSM82C55A-2		Unit	Remarks
		Min.	Max.		
Setup Time of address to the falling edge of $\overline{RD}$	t_{AR}	20		ns	Load 150 pF
Hold Time of address to the rising edge of $\overline{RD}$	t_{RA}	0		ns	
$\overline{RD}$ Pulse Width	t_{RR}	100		ns	
Delay Time from the falling edge of $\overline{RD}$ to the output of defined data	t_{RD}		120	ns	
Delay Time from the rising edge of $\overline{RD}$ to the floating of data bus	t_{DF}	10	75	ns	
Time from the rising edge of $\overline{RD}$ or $\overline{WR}$ to the next falling edge of $\overline{RD}$ or $\overline{WR}$	t_{RV}	200		ns	
Setup Time of address before the falling edge of $\overline{WR}$	t_{AW}	0		ns	
Hold Time of address after the rising edge or $\overline{WR}$	t_{WA}	20		ns	
$\overline{WR}$ Pulse Width	t_{WW}	150		ns	
Setup Time of bus data before the rising edge of $\overline{WR}$	t_{DW}	50		ns	
Holt Time of bus data after the rising edge of $\overline{WR}$	t_{WD}	30		ns	
Delay Time from the rising edge of $\overline{WR}$ to the output of defined data	t_{WB}		200	ns	
Setup Time of port data before the falling edge of $\overline{RD}$	t_{IR}	20		ns	
Hold Time of port data after the rising edge of $\overline{RD}$	t_{HR}	10		ns	
$\overline{ACK}$ Pulse Width	t_{AK}	100		ns	
$\overline{STB}$ Pulse Width	t_{ST}	100		ns	
Setup Time of port data before the rising edge of $\overline{STB}$	t_{PS}	20		ns	
Hold Time of port data after the rising edge of $\overline{STB}$	t_{PH}	50		ns	
Delay Time from the falling edge of $\overline{ACK}$ to the output of defined data	t_{AD}		150	ns	
Delay Time from the rising edge of $\overline{ACK}$ to the floating of port (Port A in mode 2)	t_{KD}	20	250	ns	
Delay Time from the rising edge of WR to the falling edge of $\overline{OBF}$	t_{WOB}		150	ns	
Delay Time from the falling edge of ACK to the rising edge of $\overline{OBF}$	t_{AOB}		150	ns	
Delay Time from the falling edge of STB to the rising edge of IBF	t_{SIB}		150	ns	
Delay Time from the rising edge of $\overline{RD}$ to the falling edge of IBF	t_{RIB}		150	ns	
Delay Time from the falling edge of $\overline{RD}$ to the falling edge of INTR	t_{RIT}		200	ns	
Delay Time from the rising edge of $\overline{STB}$ to the rising edge of INTR	t_{SIT}		150	ns	
Delay Time from the rising edge of $\overline{ACK}$ to the rising edge of INTR	t_{AIT}		150	ns	
Delay Time from the falling edge of $\overline{WR}$ to the falling edge of INTR	t_{WIT}		250	ns	

Note: Timing is measured at V_L = 0.8 V and V_H = 2.2 V for both input and outputs.

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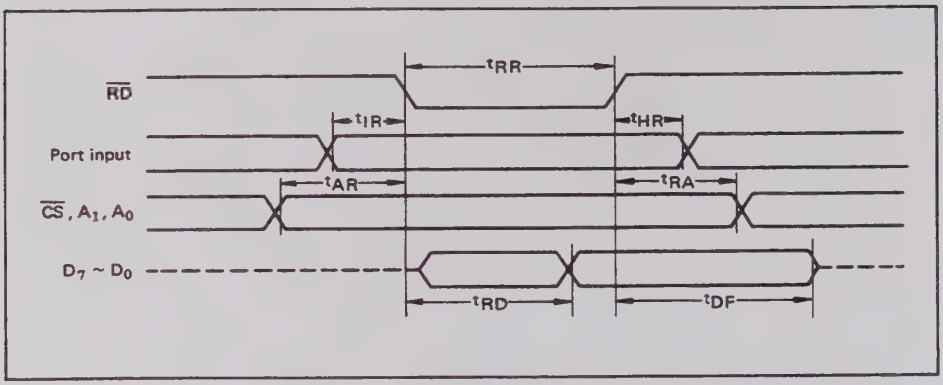
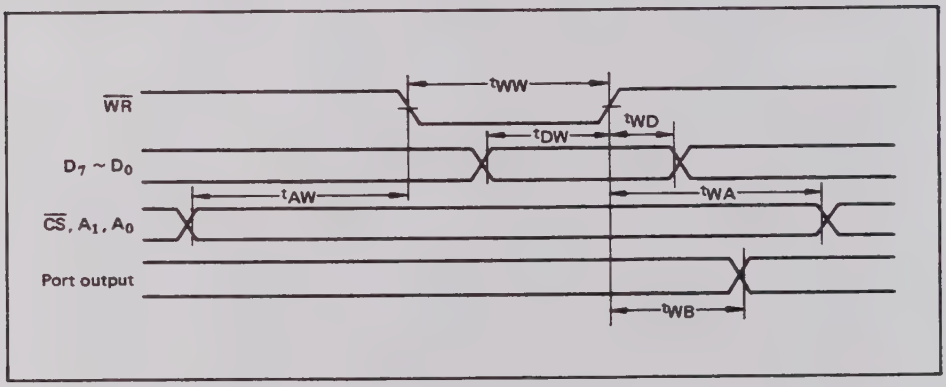
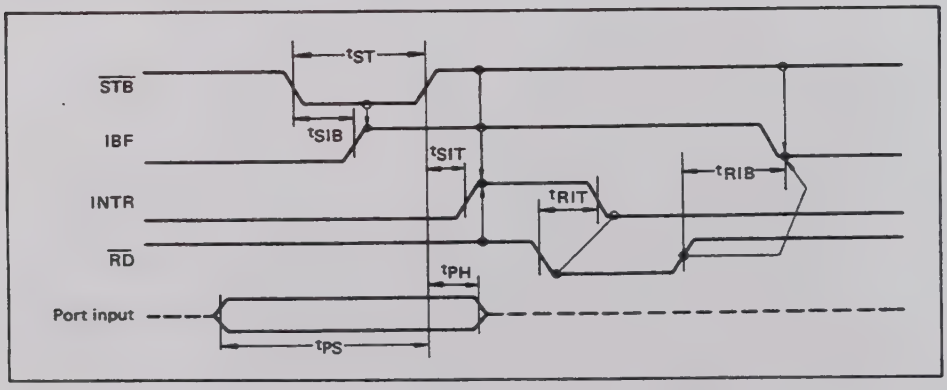
Basic Input Operation (Mode 0)



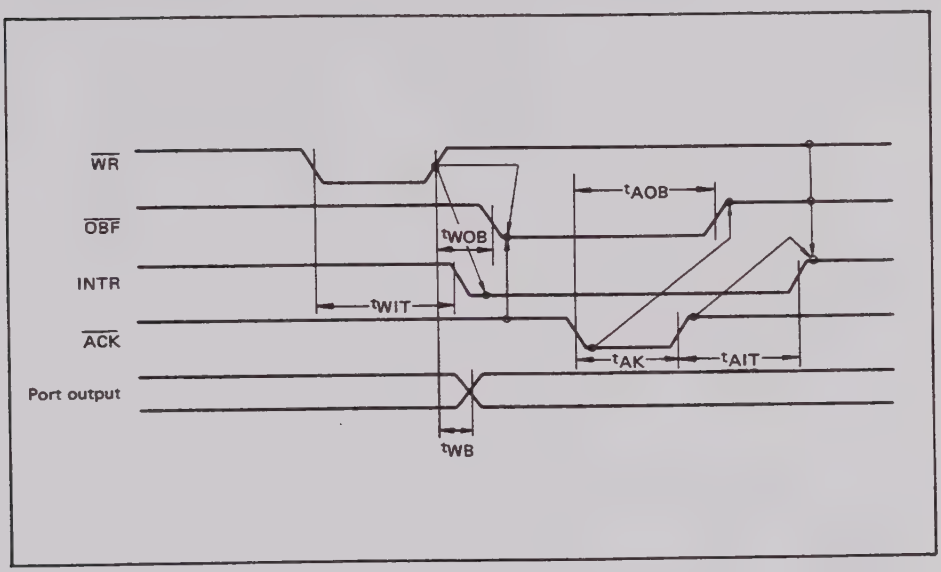
Basic Output Operation (Mode 0)



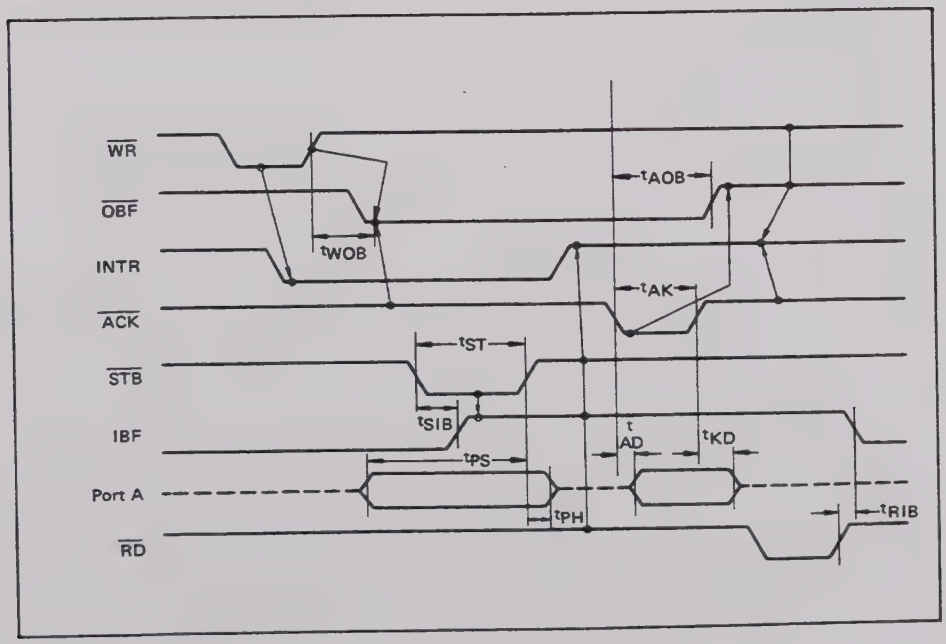
Strobe Input Operation (Mode 1)



Strobe Output Operation (Mode 1)



Bidirectional Bus Operation (Mode 2)



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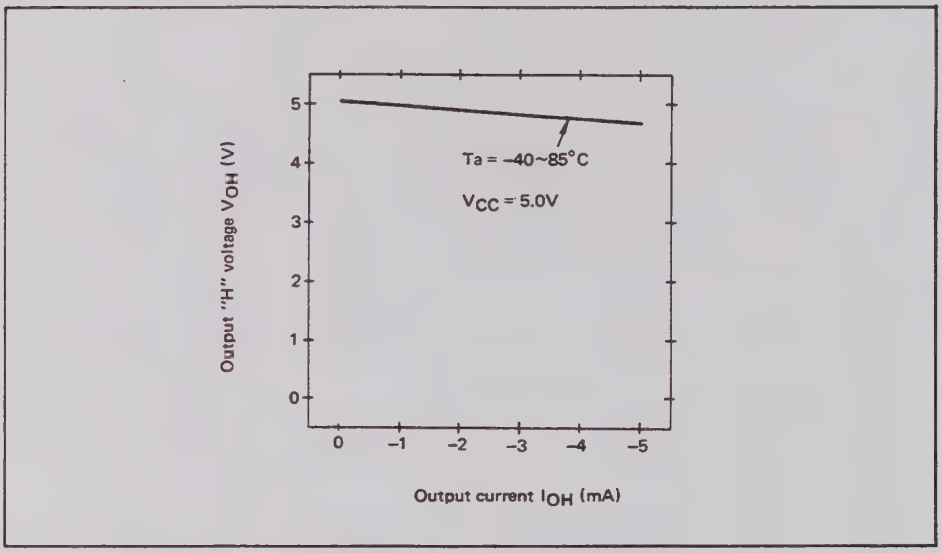
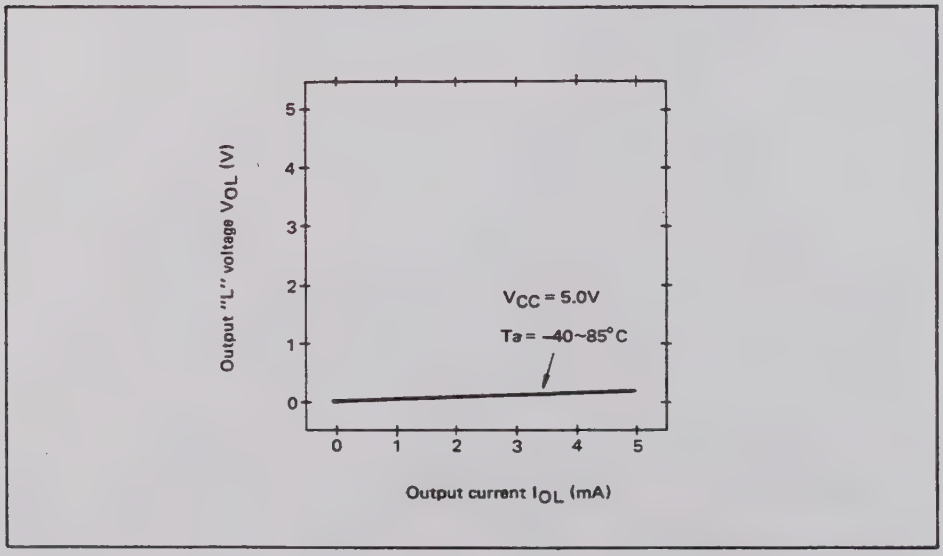
OUTPUT CHARACTERISTICS (REFERENCE VALUE)

1 Output "H" Voltage (V_{OH}) vs. Output Current (I_{OH})



2 Output "L" Voltage (V_{OL}) vs. Output Current (I_{OL})



Note: The direction of flowing into the device is taken as positive for the output current.

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FUNCTIONAL DESCRIPTION OF PIN

Pin No.	Item	Input/Output	Function
D7 ~ D0	Bidirectional data bus	Input and output	These are three-state 8-bit bidirectional buses used to write and read data upon receipt of the $\overline{WR}$ and $\overline{RD}$ signals from CPU and also used when control words and bit set/reset data are transferred from CPU to MSM82C55A.
RESET	Reset input	Input	This signal is used to reset the control register and all internal registers when it is in high level. At this time, ports are all made into the input mode (high impedance status). all port latches are cleared to 0. and all ports groups are set to mode 0.
$\overline{CS}$	Chip select input	Input	When the $\overline{CS}$ is in low level, data transmission is enabled with CPU. When it is in high level, the data bus is made into the high impedance status where no write nor read operation is performed. Internal registers hold their previous status, however.
$\overline{RD}$	Read input	Input	When RD is in low level, data is transferred from MSM82C55A to CPU.
$\overline{WR}$	Write input	Input	When WR is in low level, data or control words are transferred from CPU to MSM82C55A.
A0, A1	Port select input (address)	Input	By combination of A0 and A1, either one is selected from among port A, port B, port C, and control register. These pins are usually connected to low order 2 bits of the address bus.
PA7 ~ PA0	Port A	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word. Especially, port A can be used as a bidirectional port when it is set to mode 2.
PB7 ~ PB0	Port B	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word.
PC7 ~ PC0	Port C	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word as 2 ports with 4 bits each. When port A or port B is used in mode 1 or mode 2 (port A only), they become control pins. Especially when port C is used as an output port, each bit can be set/reset independently.
V_{CC}			+5 V power supply.
GND			GND

BASIC FUNCTIONAL DESCRIPTION

Group A and Group B

When setting a mode to a port having 24 bits, set it by dividing it into two groups of 12 bits each.

Group A: Port A (8 bits) and high order 4 bits of port C (PC7 ~ PC4)

Group B: Port B (8 bits) and low order 4 bits of port C (PC3 ~ PC0)

Mode 0, 1, 2

There are 3 types of modes to be set by grouping as follows:

Mode 0: Basic input operation/output operation (Available for both groups A and B)

Mode 1: Strobe input operation/output operation (Available for both groups A and B)

Mode 2: Bidirectional bus operation (Available for group A only)

When used in mode 1 or mode 2, however, port C has bits to be defined as ports for control signal for operation ports (port A for group A and port B for group B) of their respective groups.

Port A, B, C

The internal structure of 3 ports is as follows:

Port A: One 8-bit data output latch/buffer and one 8-bit data input latch

Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input)

Single bit set/reset function for port C

When port C is defined as an output port, it is possible to set (to turn to high level) or reset (to turn to low level) any one of 8 bits individually without affecting other bits.

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OPERATIONAL DESCRIPTION

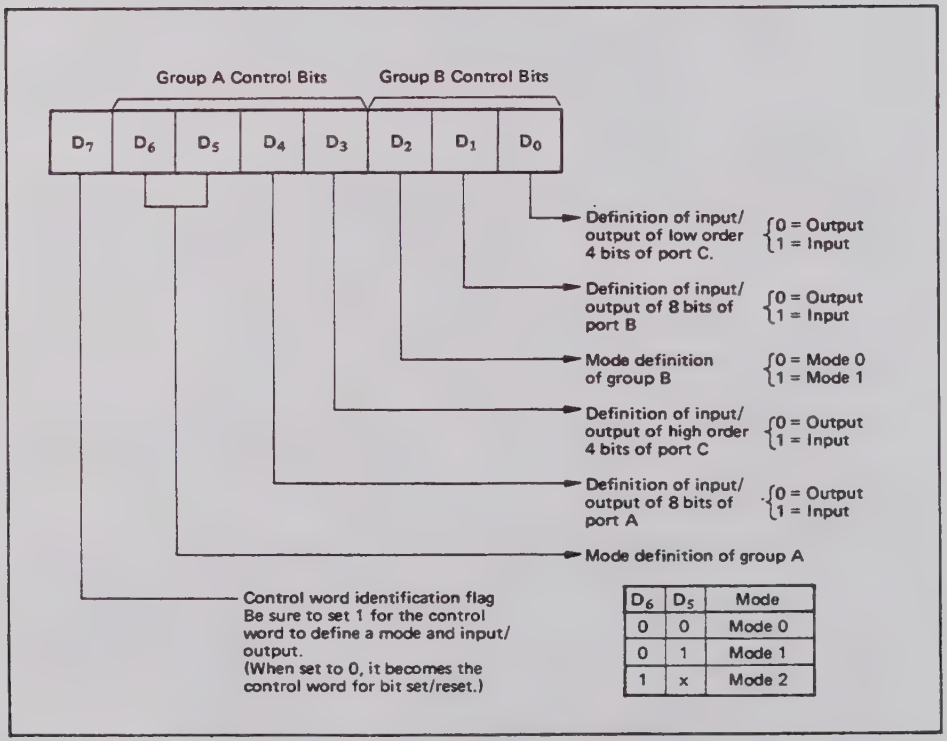
Control Logic

Operations by addresses and control signals, e.g., read and write, etc. are as shown in the table below:

Operation	A1	A0	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Operation
Input	0	0	0	1	0	Port A → Data Bus
	0	1	0	1	0	Port B → Data Bus
	1	0	0	1	0	Port C → Data Bus
Output	0	0	0	0	1	Data Bus → Port A
	0	1	0	0	1	Data Bus → Port B
	1	0	0	0	1	Data Bus → Port C
Control	1	1	0	0	1	Data Bus → Control Register
Others	1	1	0	1	0	Illegal Condition
	x	x	1	x	x	Data bus is in the high impedance status.

Setting of Control Word

The control register is composed of 7-bit latch circuit and 1-bit flag as shown below.


Group A Control Bits
Group B Control Bits
D7 D6 D5 D4 D3 D2 D1 D0
Definition of input/ output of low order 4 bits of port C. {0 = Output 1 = Input
Definition of input/ output of 8 bits of port B {0 = Output 1 = Input
Mode definition of group B {0 = Mode 0 1 = Mode 1
Definition of input/ output of high order 4 bits of port C {0 = Output 1 = Input
Definition of input/ output of 8 bits of port A {0 = Output 1 = Input
Mode definition of group A
Control word identification flag Be sure to set 1 for the control word to define a mode and input/ output. (When set to 0, it becomes the control word for bit set/reset.)

D_6	D_5	Mode
0	0	Mode 0
0	1	Mode 1
1	x	Mode 2

Precaution for mode selection

The output registers for ports A and C are cleared to ϕ each time data is written in the command register and the mode is changed, but the port B state is undefined.

Bit Set/Reset Function

When port C is defined as output port, it is possible to set (set output to 1) or reset (set output to 0) any one of 8 bits without affecting other bits as shown next page.

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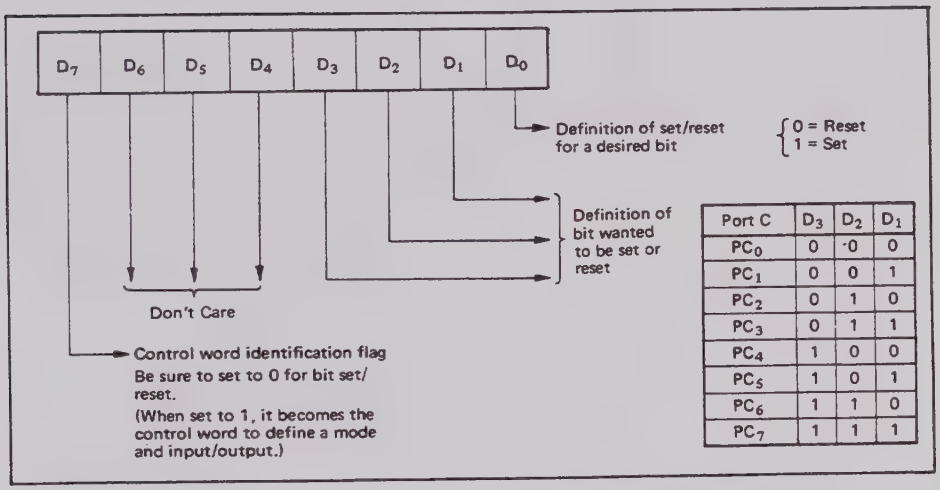
D7 D6 D5 D4 D3 D2 D1 D0
Definition of set/reset for a desired bit
0 = Reset
1 = Set
Definition of bit wanted to be set or reset
Don't Care
Control word identification flag
Be sure to set to 0 for bit set/reset.
(When set to 1, it becomes the control word to define a mode and input/output.)

Port C	D_3	D_2	D_1
PC_0	0	0	0
PC_1	0	0	1
PC_2	0	1	0
PC_3	0	1	1
PC_4	1	0	0
PC_5	1	0	1
PC_6	1	1	0
PC_7	1	1	1

Interrupt Control Function

When the MSM82C55A is used in mode 1 or mode 2, the interrupt signal for the CPU is provided. The interrupt request signal is output from port C. When the internal flip-flop INTE is set beforehand at this time, the desired interrupt request signal is output. When it is reset beforehand, however, the interrupt request signal is not output. The set/reset of the internal flip-flop is made by the bit set/reset operation for port C virtually.

Bit set → INTE is set → Interrupt allowed
Bit reset → INTE is reset → Interrupt inhibited

Operational Description by Mode

1. **Mode 0 (Basic input/output operation)**
   Mode 0 makes the MSM82C55A operate as a basic input port or output port. No control signals such as interrupt request, etc. are required in this mode. All 24 bits can be used as two-8-bit ports and two 4-bit ports. Sixteen combinations are then possible for inputs/outputs. The inputs are not latched, but the outputs are.

Type	Control Word								Group A		Group B	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Port A	High Order 4 Bits of Port C	Port B	Low Order 4 Bits of Port C
1	1	0	0	0	0	0	0	0	Output	Output	Output	Output
2	1	0	0	0	0	0	0	1	Output	Output	Output	Input
3	1	0	0	0	0	0	1	0	Output	Output	Input	Output
4	1	0	0	0	0	0	1	1	Output	Output	Input	Input
5	1	0	0	0	1	0	0	0	Output	Input	Output	Output
6	1	0	0	0	1	0	0	1	Output	Input	Output	Input
7	1	0	0	0	1	0	1	0	Output	Input	Input	Output
8	1	0	0	0	1	0	1	1	Output	Input	Input	Input
9	1	0	0	1	0	0	0	0	Input	Output	Output	Output
10	1	0	0	1	0	0	0	1	Input	Output	Output	Input
11	1	0	0	1	0	0	1	0	Input	Output	Input	Output
12	1	0	0	1	0	0	1	1	Input	Output	Input	Input
13	1	0	0	1	1	0	0	0	Input	Input	Output	Output
14	1	0	0	1	1	0	0	1	Input	Input	Output	Input
15	1	0	0	1	1	0	1	0	Input	Input	Input	Output
16	1	0	0	1	1	0	1	1	Input	Input	Input	Input

Note: When used in mode 0 for both groups A and B

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2. Mode 1 (Strobe input/output operation)

In mode 1, the strobe, interrupt and other control signals are used when input/output operations are made from a specified port. This mode is available for both groups A and B. In group A at this time, port A is used as the data line and port C as the control signal.

Following is a descrption of the input operation in mode 1.

$\overline{STB}$ (Strobe input)

- When this signal is low level, the data output from terminal to port is fetched into the internal latch of the port. This can be made independent from the CPU, and the data is not output to the data bus until the RD signal arrives from the CPU.

IBF (Input buffer full flag output)

- This is the response signal for the $\overline{STB}$. This signal when turned to high level indicates that data is fetched into the input latch. This signal turns to high level at the falling edge of $\overline{STB}$ and to low level at the rising edge of $\overline{RD}$.

INTR (Interrupt request output)

- This is the interrupt request signal for the CPU of the data fetched into the input latch. It is indicated by high level only when the internal INTE flip-flop is set. This signal turns to high level at the rising edge of the $\overline{STB}$ (IBF = 1 at this time) and low level at the falling edge of the $\overline{RD}$ when the INTE is set.

$INTE_A$ of group A is set when the bit for PC_4 is set, while $INTE_B$ of group B is set when the bit for PC_2 is set.

Following is a description of the output operation of mode 1.

$\overline{OBF}$ (Output buffer full flag output)

- This signal when turned to low level indicates that data is written to the specified port upon receipt of the $\overline{WR}$ signal from the CPU. This signal turns to low level at the rising edge of the WR and high level at the falling edge of the ACK.

$\overline{ACK}$ (Acknowledge input)

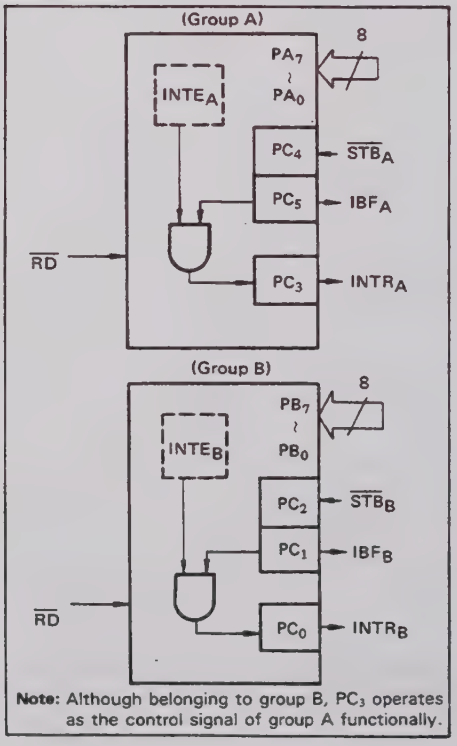
- This signal when turned to low level indicates that the terminal has received data.

INTR (Interrupt request output)

- This is the signal used to interrupt the CPU when a terminal receives data from the CPU via the MSM82C55A-5. It indicates the occurrence of the interrupt in high level only when the internal INTE flip-flop is set. This signal turns to high level at the rising edge of the $\overline{ACK}$ (OBF = 1 at this time) and low level at the falling edge of $\overline{WR}$ when the $INTE_B$ is set.

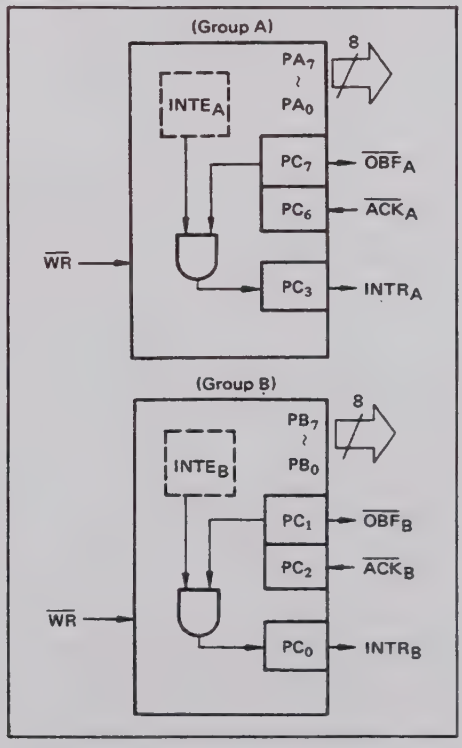
$INTE_A$ of group A is set when the bit for PC_6 is set, while $INTE_B$ of group B is set when the bit for PC_2 is set.

Mode 1 Input



Note: Although belonging to group B, PC_3 operates as the control signal of group A functionally.

Mode 1 output

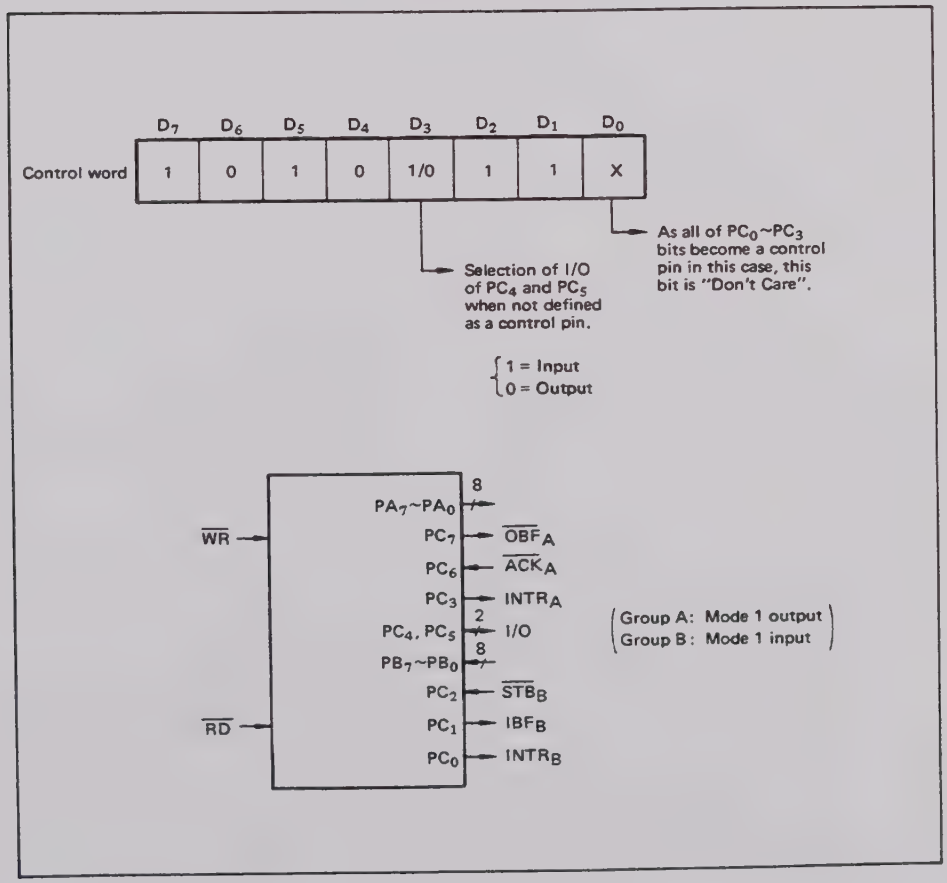


Port C Function Allocation in Mode 1

Combination of Input/Output / Port C	Group A: Input Group B: Input	Group A: Input Group B: Output	Group A: Output Group B: Input	Group A: Output Group B: Output
PC_0	$INTR_B$	$INTR_B$	$INTR_B$	$INTR_B$
PC_1	IBF_B	$\overline{OBF}_B$	IBF_B	$\overline{OBF}_B$
PC_2	$\overline{STB}_B$	$\overline{ACK}_B$	$\overline{STB}_B$	$\overline{ACK}_B$
PC_3	$INTR_A$	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	$\overline{STB}_A$	$\overline{STB}_A$	I/O	I/O
PC_5	IBF_A	IBF_A	I/O	I/O
PC_6	I/O	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	I/O	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

Note: I/O is a bit not used as the control signal, but it is available as a port of mode 0.

Examples of the relation between the control words and pins when used in mode 1 is shown below:
(a) When group A is mode 1 output and group B is mode 1 input.


D7 D6 D5 D4 D3 D2 D1 D0
Control word
1 0 1 0 1/0 1 1 X
As all of PC0~PC3 bits become a control pin in this case, this bit is "Don't Care".
Selection of I/O of PC4 and PC5 when not defined as a control pin.
1 = Input
0 = Output
8
PA7~PA0
WR
PC7 → OBFA
PC6 ← ACKA
PC3 → INTRA
2
PC4, PC5 I/O
8
PB7~PB0
PC2 → STBB
RD
PC1 → IBFB
PC0 → INTRB
Group A: Mode 1 output
Group B: Mode 1 input

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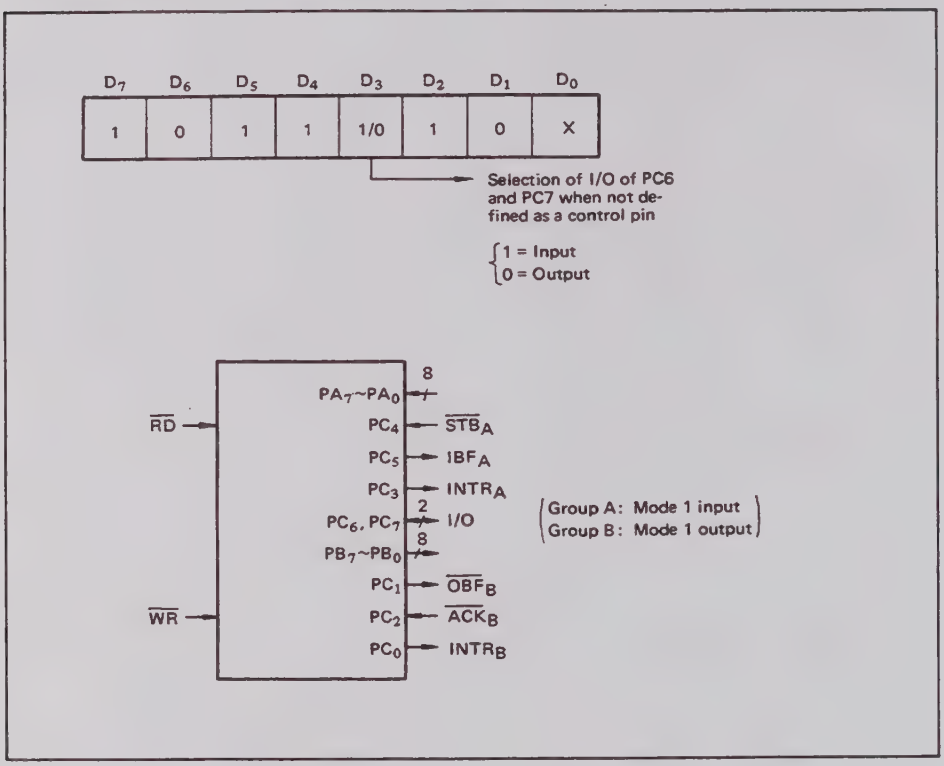
(b) When group A is mode 1 input and group B is mode 1 output.



3. Mode 2 (Strobe bidirectional bus I/O operation)

In mode 2, it is possible to transfer data in 2 directions through a single 8-bit port. This operation is akin to a combination between input and output operations. Port C waits for the control signal in this case, too. Mode 2 is available only for group A, however.

Next, a description is made on mode 2.

$\overline{OBF}$ (Output buffer full flag output)

- This signal when turned to low level indicates that data has been written to the internal output latch upon receipt of the $\overline{WR}$ signal from the CPU. At this time, port A is still in the high impedance status and the data is not yet output to the outside. This signal turns to low level at the rising edge of the $\overline{WR}$ and high level at the falling edge of the $\overline{ACK}$.

$\overline{ACK}$ (Acknowledge input)

- When a low level signal is input to this pin, the high impedance status of port A is cleared, the buffer is enabled, and the data written to the internal output latch is output to port A. When the input returns to high level, port A is made into the high impedance status.

$\overline{STB}$ (Strobe input)

- When this signal turns to low level, the data output to the port from the pin is fetched into the internal input latch. The data is output to the data bus upon receipt of the RD signal from the CPU, but it remains in the high impedance status until then.

IBF (Input buffer full flag output)

- This signal when turned to high level indicates that data from the pin has been fetched into the input latch. This signal turns to high level at the falling edge of the $\overline{STB}$ and low level at the rising edge of the $\overline{RD}$.

INTR (Interrupt request output)

- This signal is used to interrupt the CPU and its operation in the same as in mode 1. There are two INTE flip-flops internally available for input and output to select either interrupt of input or output operation. The INTE1 is used to control the interrupt request for output operation and it can be reset by the bit set for PC6. INTE2 is used to control the interrupt request for the input operation and it can be set by the bit set for PC4.

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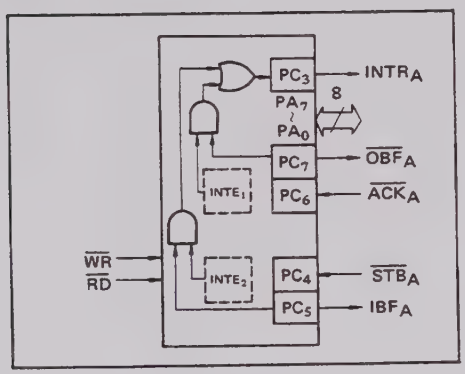
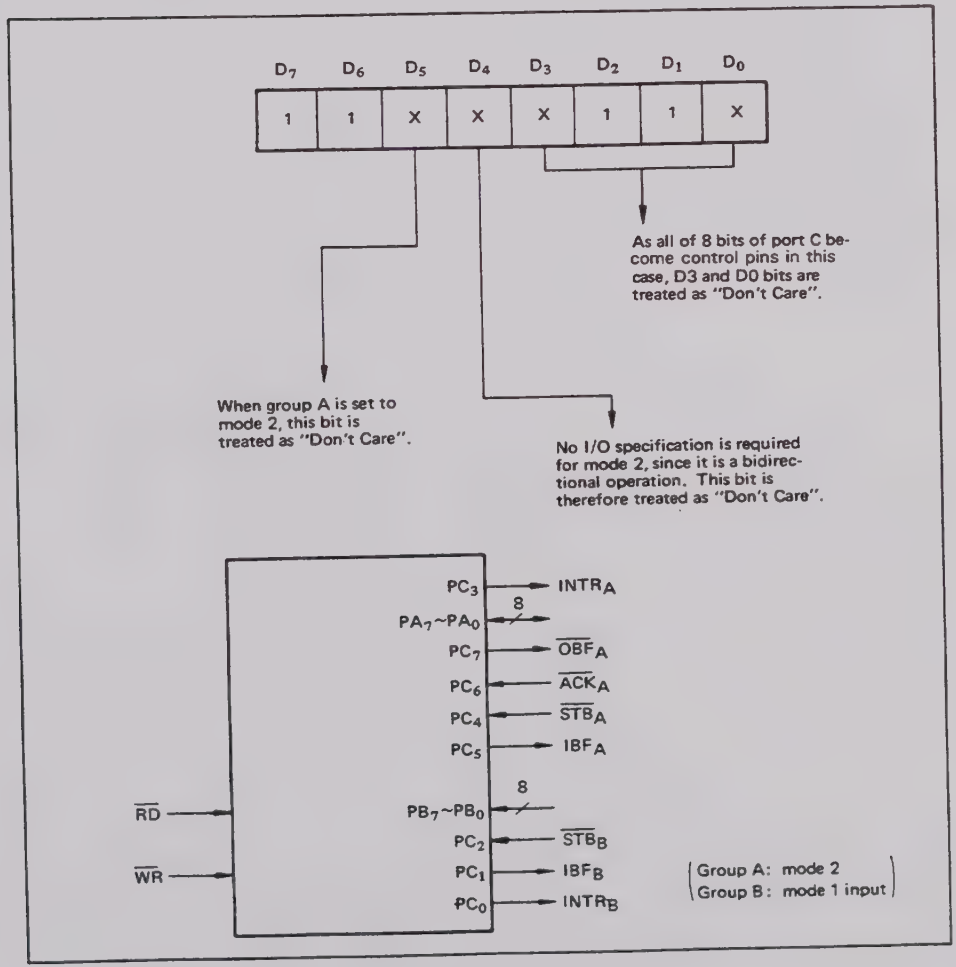
Mode 2 I/O Operation



Port C Function Allocation in Mode 2

Port C	Function
PC_0	Confirmed to the group B mode
PC_1	
PC_2	
PC_3	$INTR_A$
PC_4	$\overline{STB}_A$
PC_5	IBF_A
PC_6	$\overline{ACK}_A$
PC_7	$\overline{OBF}_A$

Following is an example of the relation between the control word and the pin when used in mode 2. When input in mode 2 for group A and in mode 1 for group B.



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4. When Group A is Different in Mode from Group B

Group A and group B can be used by setting them in different modes each other at the same time. When either group is set to mode1 or mode 2, it is possible to set the one not defined as a control pin in port C to both input and output as a port which operates in mode 0 at the 3rd and 0th bits of the control word.

(Mode combinations that define no control bit at port C)

	Group A	Group B	Port C							
			PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0
1	Mode 1 input	Mode 0	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	I/O	I/O	I/O
2	Mode 0 output	Mode 0	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	I/O	I/O	I/O
3	Mode 0	Mode 1 input	I/O	I/O	I/O	I/O	I/O	$\overline{STB}_B$	IBF_B	$INTR_B$
4	Mode 0	Mode 1 output	I/O	I/O	I/O	I/O	I/O	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
5	Mode 1 input	Mode 1 input	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$
6	Mode 1 input	Mode 1 output	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
7	Mode 1 output	Mode 1 input	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$
8	Mode 1 output	Mode 1 output	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
9	Mode 2	Mode 0	$\overline{OBF}_A$	$\overline{ACK}_A$	IBF_A	$\overline{STB}_A$	$INTR_A$	I/O	I/O	I/O
			Controlled at the 3rd bit (D3) of the control word				Controlled at the 0th bit (D0) of the control word			

When the I/O bit is set to input in this case, it is possible to access data by the normal port C read operation.
When set to output, PC7 ~ PC4 bits can be accessed by the bit set/reset function only. Meanwhile, 3 bits from PC2 to PC0 can be accessed by normal write operation.

The bit set/reset function can be used for all of PC3 ~ PC0 bits. Note that the status of port C varies according to the combination of modes like this.

5. Port C Status Read

When port C is used for the control signal, that is, in either mode 1 or mode 2, each control signal and bus status signal can be read out by reading the content of port C.
The status read out is as follows:

	Group A	Group B	Status read on the data bus							
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	Mode 1 input	Mode 0	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	I/O	I/O	I/O
2	Mode 1 output	Mode 0	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	I/O	I/O	I/O
3	Mode 0	Mode 1 input	I/O	I/O	I/O	I/O	I/O	$INTE_B$	IBF_B	$INTR_B$
4	Mode 0	Mode 1 output	I/O	I/O	I/O	I/O	I/O	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
5	Mode 1 input	Mode 1 input	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
6	Mode 1 input	Mode 1 output	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
7	Mode 1 output	Mode 1 input	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
8	Mode 1 output	Mode 1 output	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
9	Mode 2	Mode 0	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	I/O	I/O	I/O
10	Mode 2	Mode 1 input	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
11	Mode 2	Mode 1 output	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$

6. Reset of MSM82C55A

Be sure to keep the RESET signal at power ON in the high level at least for 50 μs. Subsequently, it becomes the input mode at a high level pulse above 500 ns.

Note: Comparison of MSM82C55A-5 and MSM82C55A-2

MSM82C55A-5

After a write command is executed to the command register, the internal latch is cleared in PORTA PORTC. For instance, 00H is output at the beginning of a write command when the output port is assigned. However, if PORTB is not cleared at this time, PORTB is unstable. In other words, PORTB only outputs ineffective data (unstable value according to the device) during the period from after a write command is executed till the first data is written to PORTB.

MSM82C55A-2

After a write command is executed to the command register, the internal latch is cleared in All Ports(PORTA,PORTB,PORTC). 00H is ontput at the beginning of a write command when the output port is assigned.

Appendix D
Customer Communication

For your convenience, this appendix contains forms to help you gather the information necessary to help us solve technical problems you might have as well as a form you can use to comment on the product documentation. Filling out a copy of the *Technical Support Form* before contacting National Instruments helps us help you better and faster.

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Netherlands	03480 33466	03480 30673
Norway	32 84 84 00	32 84 86 00
Singapore	2265886	2265887
Spain	91 640 0085	91 640 0533
Sweden	08 730 49 70	08 730 43 70
Switzerland	056 20 51 51	056 20 51 55
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Fax (___)_____ Phone (___)_____

Computer brand _____ Model _____ Processor _____

Operating system _____

Speed _____MHz RAM _____MB Display adapter _____

Mouse _____yes _____no Other adapters installed _____

Hard disk capacity _____MB Brand _____

Instruments used _____

National Instruments hardware product model _____ Revision _____

Configuration _____

National Instruments software product _____ Version _____

Configuration _____

The problem is _____

_____

_____

_____

_____

List any error messages _____

_____

_____

_____

_____

The following steps will reproduce the problem _____

_____

_____

PC-DIO-24 Hardware and Software Configuration Form

Record the settings and revisions of your hardware and software on the line to the right of each item. Complete a new copy of this form each time you revise your software or hardware configuration, and use this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

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- PC-DIO-24 Revision _____
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- Interrupt Enable Line of PC-DIO-24 (Factory Setting–PC4) _____
- Interrupt Level of PC-DIO-24 (Factory Setting–5) _____
- Handshaking Mode (mode 0, mode 1, mode 2) _____
- NI-DAQ or LabWindows/CVI Version _____

Other Products

- Computer Make and Model _____
- Microprocessor _____
- Clock Frequency _____
- Type of Video Board Installed _____
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Glossary

Prefix	Meaning	Value
μ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}

°	degrees
Ω	ohms
%	percent
A	amperes
AWG	American Wire Gauge
BCD	binary-coded decimal
C	Celsius
DMA	direct memory access
hex	hexadecimal
Hz	hertz
in.	inches
Iin	input current
Iout	output current
kbytes	1,024 bytes
LSB	least significant bit
MB	megabytes of memory
m	meters
MSB	most significant bit
PPI	programmable peripheral interface
R_{EXT}	external resistance
s	seconds
SSR	solid-state relay
V	volts
V_{EXT}	external volt
VDC	volts direct current

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